# A Novel "In-Situ" Processed Gate Region on GaN MOS Capacitors

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# Abstract

This work reports a route to the realisation of GaN metal oxide semiconductor capacitors (MOSCAPs) where the GaN surface has not been exposed to atmosphere. This has been achieved by the deposition of a 5nm $SiN_x$ "capping" layer as the final part of the GaN on Si MOSCAP wafer growth to encapsulate the GaN surface, followed by its removal in a "cluster" plasma processing tool, which enables both etching of samples and subsequent dielectric and metal deposition without atmospheric exposure between process steps. Capacitance-voltage hysteresis, $\Delta_{Hysteresis,}$ of 90mV and frequency dispersion, $\Delta_{Dispersion}$, of 150mV were achieved from samples where the $SiN_x$ capping layer was etched and then transferred under vacuum prior to atomic layer deposition (ALD) of a 20 nm $Al_2O_3$ gate dielectric. These were lower than the previously reported values of 250mV and 350mV respectively for GaN-$Al_2O_3$ MOS capacitors where the GaN surface had been exposed to atmosphere. The effects of $N_2$ and $H_2$ plasma treatments after $SiN_x$ etch and prior to $Al_2O_3$ deposition were examined. Exposure to a 150W $N_2$ plasma for 5 minutes produced $\Delta_{Hysteresis}$ and $\Delta_{Dispersion}$ of 200mV and 250mV respectively, both of which reduced to 60mVafter forming gas annealing (FGA) in 10% $H_2$/90% $N_2$ for 30 minutes at 430$^o$C. The insertion of an ALD grown AlN interlayer between an air exposed GaN surface and the $Al_2O_3$ gate dielectric resulted in 50mV $\Delta_{Hysteresis}$ and $\Delta_{Dispersion}$. However, when the process was transferred to samples that went through the $SiN_x$ etch and optimised $N_2$ plasma pretreatment, both $\Delta_{Hysteresis}$ and $\Delta_{Dispersion}$ increased to 500mV. The effect of ALD deposition of a TiN gate metal after $Al_2O_3$ gate dielectric was also examined. $SiN_x$ capped samples were first etched in the cluster tool before transfer to the ALD chamber in which a 20nm $Al_2O_3$ gate dielectric was deposited. This was followed by atomic layer deposition of 20nm TiN gate metal. $\Delta_{Hysteresis}$ and $\Delta_{Dispersion}$ of 550mV and 400mV respectively were obtained. These samples had a capacitance-voltage slope which was 155% higher than otherwise comparable structures with Pt/Au gate metal. In conclusion the reductions in $\Delta_{Hysteresis}$ and $\Delta_{Dispersion}$ achieved in this work during in-situ etching and ALD are encouraging for the realisation of high power GaN devices.

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# Associated Publications

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Floros, K., Li, X. , Guiney, I., Cho, S.-J., **Hemakumara, D.**, Wallis, D. J., Wasige, E. , Moran, D. A.J., Humphreys, C. J. and Thayne, I. G., "Dual barrier InAlN/AlGaN/GaN-on-silicon high-electron-mobility transistors with Pt and Ni based gate stacks.", *Physica Status Solidi A: Applications and Materials Science*, 214(8), 1600835 (2017).

**Hemakumara, D**, Li, X., Floros, K., Cho S. J., Guiney, I., Moran, D., Humphreys, C., O'Mahony, A., Knoops, H., and Thayne, I., G., "The impact on GaN MOS Capacitor Performance of in-situ processing in a clustered ALD/ICP/RIE tool ", 17$^{th}$ International Conference on Atomic Layer Deposition, Dencer, USA July 15-18, 2017.

**Hemakumara, D**, Li, X., Floros, K., Cho S. J., Guiney, I., Moran, D., Humphreys, C., O'Mahony, A., Knoops, H., and Thayne, I., G., "4x reduction in GaN MOS capacitor flatband voltage hysteresis by using an in-situ deposited SiNx capping layer and device processing in a cluster tool", 12$^{th}$ International Conference on Nitride Semiconductors, Strasbourg, France July 23-28, 2017.

# 1. Introduction

## 1.1 Background

Today's society relishes the comforts of communication, transport, light and other tangible benefits thanks to the production of electrical energy. Currently electrical energy amounts to 40% of worldwide energy consumption [1]. However, because humankind relies greatly on its usage, we are currently faced with two significant obstacles [2]. Firstly, due to the increase in population the energy consumption is expected to rise by 48% within the next 30 years [3]. Secondly, the rise in levels of carbon dioxide in the atmosphere as a consequence of the higher energy usage can result in climate change, the adverse effects of which include damage to vegetation, the melting of polar ice caps and loss of habitats for wildlife. Therefore, ways of mitigating the effects of these obstacles is of utmost importance [4].

The USA currently has the highest per capita emission of $CO_2$ in the world, as Illustrated in Figure 1.1.1, which shows an energy flow diagram from 2016 displaying the sources of electricity on the left hand side and the end-use energy consumption on the right hand side [5]. It can be seen that from electricity generation to its utilisation, out of the 37.5 quadrillion British thermal units (quads) of energy consumed, 24.9 quads of it has been rejected. Therefore 66.4% of energy has been wasted, making electricity generation only 33.6% efficient. It can also be observed from Figure 1.1.1 that the majority of energy produced to date is generated by burning fossil fuels, which are the biggest contributors to atmospheric $CO_2$ increase. Lastly, the USA's total energy consumption amounts to 97.2 quads with a total energy rejection amounting to 66.4 quads, i.e., more than half the energy generated (68.2%) has been wasted. Thus, to reduce such high power wastage and to keep $CO_2$ emissions to a minimum, considerable improvements should be made, from the sources of electricity generation to power delivery and conversion.

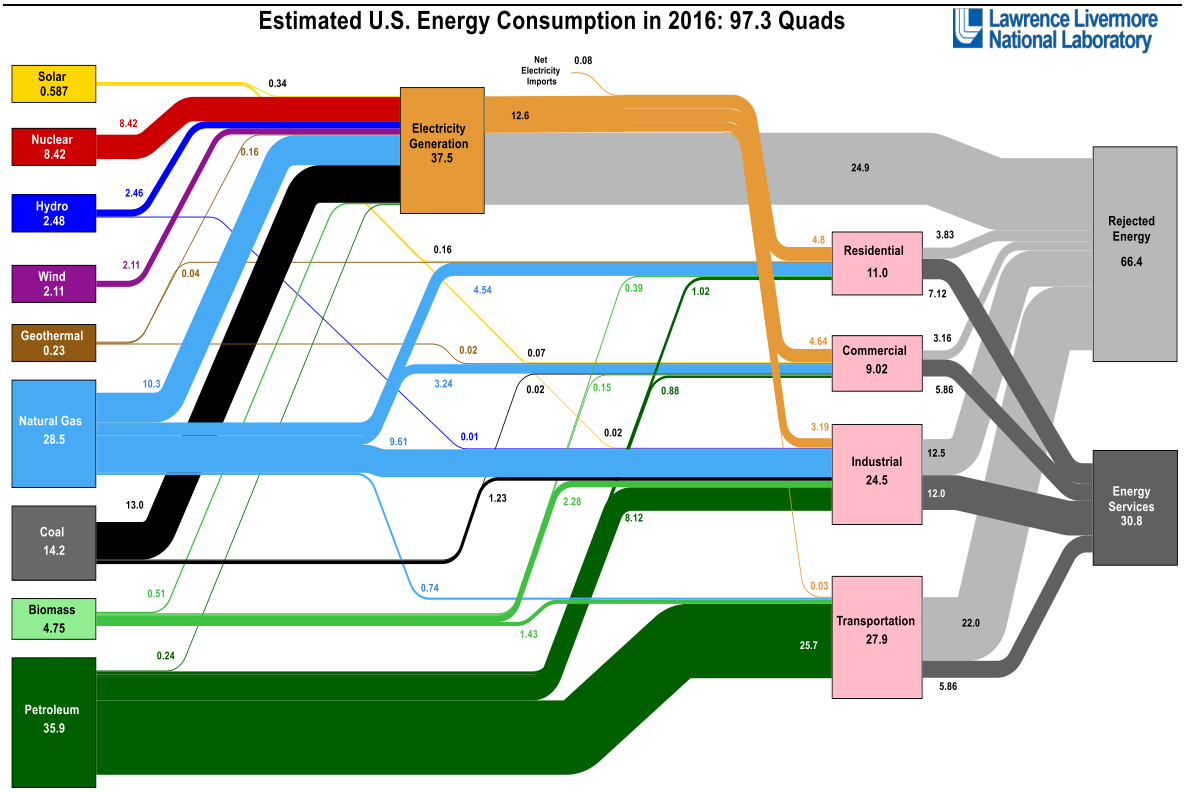



**Figure 1.1.1:** Energy Flow chart [5]

The usage of cleaner renewable energy sources such as wind and solar, replacement of incandescent lights with light emitting diodes (LEDs) and use of environmentally friendly electric vehicles can assist in reducing the emission of $CO_2$ [6]. However, before electricity reaches the end user it goes through various power electronic converters. These converters are enabled by devices that fall under the branch of engineering known as power electronics. Power electronics are responsible for controlling and conditioning electrical energy from the source to the load. Thus, advancements of these technologies play a critical role in increasing further the efficiency of energy conversion. Through the widespread adoption of efficient load architectures that are controlled by power electronics it is predicted that a 25% decrease in the worldwide annual energy consumption can be made [6].

The operation of a power electronic device is essentially that of a switch and operates between an ON and OFF state. During the application of a voltage the device turns ON and conducts current through it. The main energy losses associated with a power electronic device are switching losses and conduction losses. Switching loses occur during transitions,

when the device is being turned OFF or ON, and conduction losses occur during the ON or OFF state. Advancements in reducing these losses is key to energy efficient power conversion.

## 1.2 Comparison of semiconductor material

To date Silicon transistors have been the most widely used devices in power electronics. However, research on wide band gap (WBG) materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) show they have the fundamental properties that suggest power transistors realised from these materials will be able to surpass the performance of Si-based devices. Table 1.2.1 summarises a comparison between the properties of silicon and other semiconductor materials.

| Semiconductor Material | Band gap eV | Electron Mobility $\mu$ $cm^2/V\text{-}s$ | Hole Mobility $\mu$ $cm^2/V\text{-}s$ | Relative Dielectric constant $\varepsilon$ | Critical Electric Field $E_{cl}$ (MV/cm) | Baliga Figure of Merit BFOM |
|---|---|---|---|---|---|---|
| Si | 1.12 | 1360 | 480 | 11.7 | 0.3 | 1 |
| GaAs | 1.43 | 8500 | 400 | 13.1 | 0.4 | 17 |
| SiC | 3.26 | 700 | 120 | 9.7 | 2.2 | 134 |
| GaN | 3.45 | 900<br>1880-2000[a] | 200 | 8.9 | 3.3 | 537<br>1480[a] |

**Table 1.2.1:** Comparison of material properties between silicon [7]
[a] Electron mobility when used in heterostructure

These material parameters can be translated in to an estimation of device characteristics by calculating their theoretical performances, which are discussed in detail below. However, it is important that the basic operation of a field effect transistor (FET), a key power electronics component, and its architecture be defined. Figure 1.2.1 illustrates the cross-section of a GaN-based FET, further details of the layer structure will be discussed in section 3. The device contains three terminals; namely source, drain and gate and a conducting channel through which carriers flow from the source to the drain. A current flow in the channel is created when a voltage is applied between the source and the drain, $V_{ds}$ and the flow of carriers beneath the gate is controlled by the voltage applied at the gate terminal, $V_{gs}$.

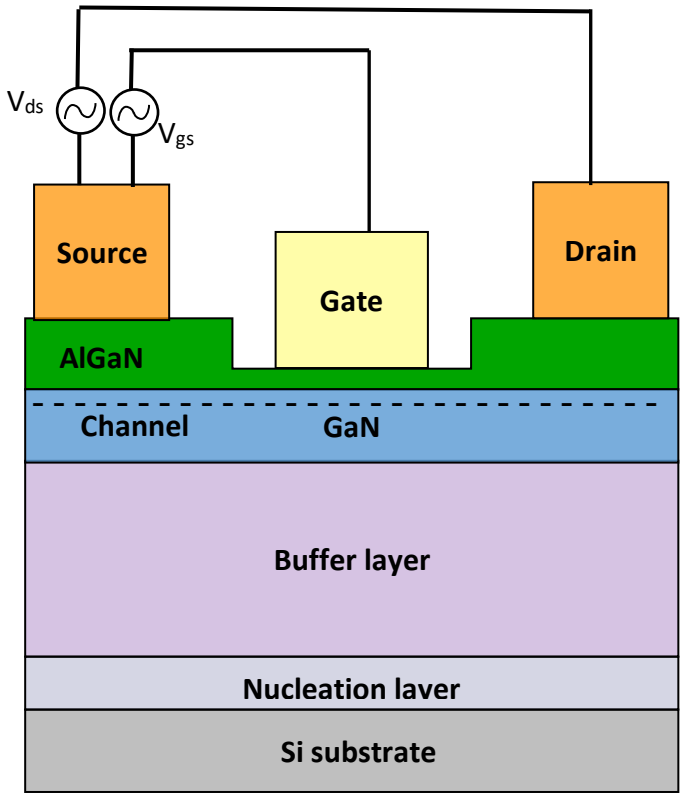



**Figure 1.2.1: Cross-section of a transistor**

### 1.2.1 Breakdown voltage

Breakdown voltage is the maximum allowable voltage that a device can sustain. It occurs when the electric field applied reaches the critical electric field and is brought about by the onset of impact ionisation [8]. It is the phenomenon where electron-hole pairs are generated as a result of energy gained from the electric field. These pairs participate in the creation of additional pairs and the process continues eventually leading to a large and uncontrolled current flow. This results in the device unable to sustain a further increase in the applied voltage and is said to undergo avalanche breakdown [8].

As seen in table 1.2.1, gallium nitride has a critical electric field that is approximately 10 times that of silicon and is therefore able to reach higher breakdown voltages.

### 1.2.2 Efficiency

**1.2.2(a)** Devices realised with gallium nitride are capable of achieving high conversion efficiency due to the low conduction losses arising from them. The power loss during conduction is shown in equation 1.1. The on-resistance of the transistor, ($R_{DS(on)}$) is the resistance between the terminals when the transistor is conducting. To reduce the

conduction losses, it is essential that $R_{DS_{(on)}}$ is minimised. Expressed in equation 1.2 is the formula for the theoretical $R_{DS_{(on)}}$ of the transistor, of which the denominator is known as the Baliga figure of merit (BFOM) and it is indicative of the conduction losses. A higher BFOM results in lower $R_{DS(on)}$. GaN has the highest BFOM when compared to the other materials presented in table 1 and therefore in theory would produce the lowest on resistance and hence the lowest conduction losses.

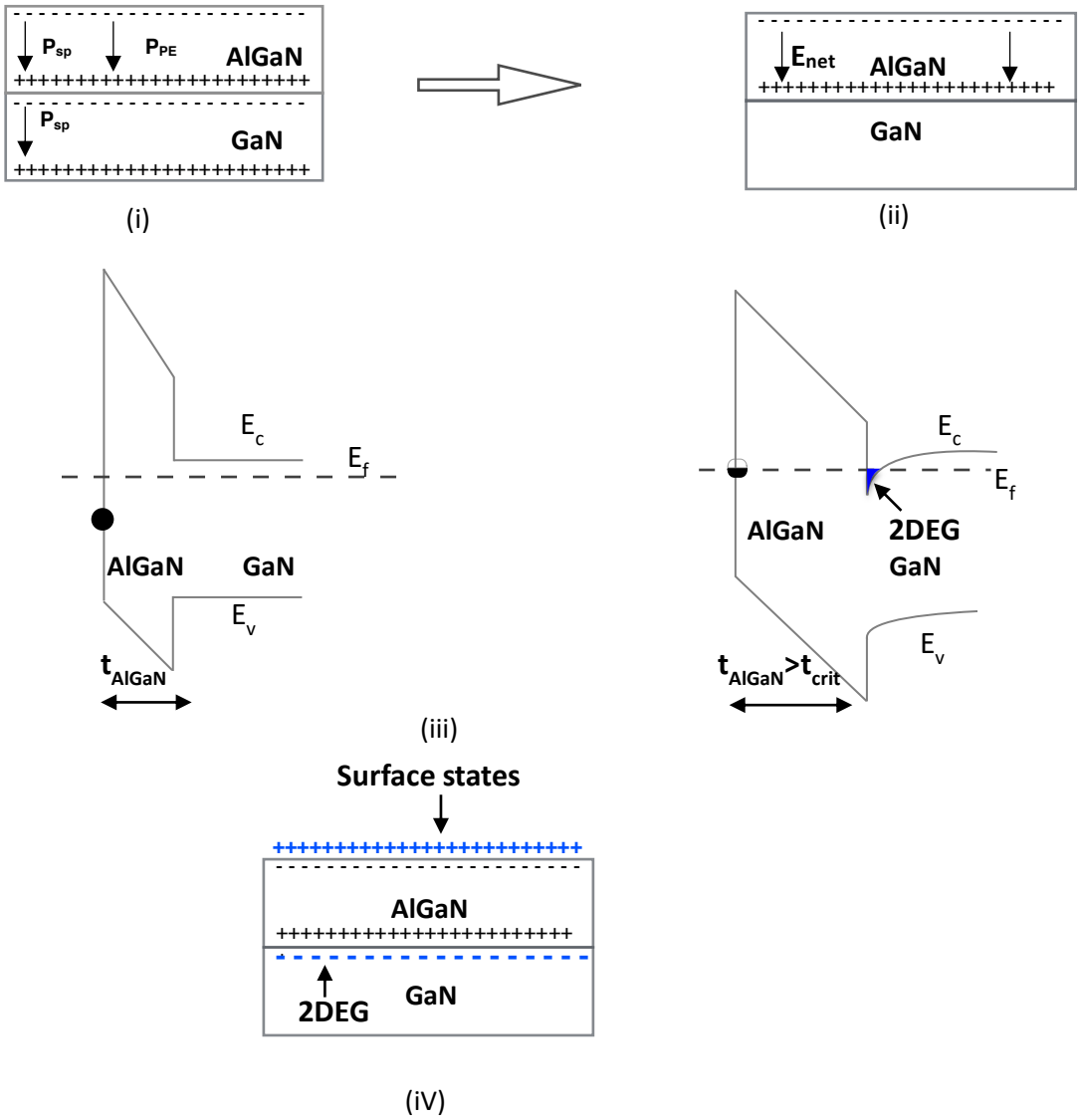
$$P_{diss} = I_d{}^2 R_{DS_{on}} \quad [9] \qquad 1.1$$

$$R_{DS_{(on)}} = BV^2/q\mu Q_s E^2{}_{cl} \quad [10] \qquad 1.2$$

$P_{diss} = \text{Power dissipation},\ I_d = \text{Drain current},$
$R_{DS_{on}} = \text{On} - \text{resistance},\ BV = \text{Breakdown voltage},\ q = \text{charge}, \mu = \text{mobility}, E_{cl} = \text{Critical electric field}, Q_S = \text{sheet carier density}$

**1.2.2(b)** The carrier concentration and mobility of GaN based devices can be further increased compared to bulk GaN by incorporating a heterostructure with an undoped layer of AlGaN grown on GaN. This is a result of a high electron concentration at the AlGaN/GaN interface that occurs due to their material properties [11]. A spontaneous polarisation ($P_{SP}$) exists in both the materials and is a consequence of the high electronegativity of nitrogen that causes sheet charge densities of opposing polarity to exist in the crystal as illustrated in Figure 1.2.2 1(i)**.** The AlGaN layer when grown on GaN is strained due to the difference in the lattice constants between these materials, causing a piezoelectric polarisation ($P_{PE}$) to occur and this contributes to another sheet charge density in AlGaN. This give rise to the net electric field, $E_{net}$ shown in Figure 1.2.2.1(ii)**.** The surface of a non-ideal AlGaN consists of donor-like states [12]. If the AlGaN layer thickness ($t_{AlGaN}$) is greater than some critical value ($t_{crit}$), the surface states reach the Fermi level to compensate the net electric field present as shown in Figure 1.2.2.1(iii) and (iv). Electrons are then transferred from the occupied surface states to the conduction band at the interface. The confinement of electrons in a quantum well separates spatially the carriers from the ionised donors. This results in the increase in mobility of the carriers because they are not affected by ionised impurity scattering. The increase in carrier concentration and mobility is illustrated in the graph shown in Figure 1.2.2.2 The resulting channel of electrons is 2 dimensional because the thickness of this channel is much lower in comparison to its length and width, hence it is named a 2 dimensional electron gas (2DEG). Thus, the existence of the 2DEG with highly

mobile carriers gives rise to a high electron mobility transistor (HEMT). The increase in mobility of the charge carriers further reduces $R_{ON}$ as can be seen on equation 2.2.2.




**$E_c$= Conduction band, $E_v$= Valence band, $E_f$= Fermi level, $E_{net}$= Net electric field, $t_{AlGaN}$= Thickness of AlGaN, $t_{crit}$= Critical thickness**

**Figure 1.2.2.1 (i)** Spontaneous and piezoelectric induced charges, **(ii)** Net polarization charge **(iii)** Band Diagram of AlGaN/GaN before and after critical thickness is reached **(iv)** AlGaN/ GaN with net polarization charge, surface states and 2DEG

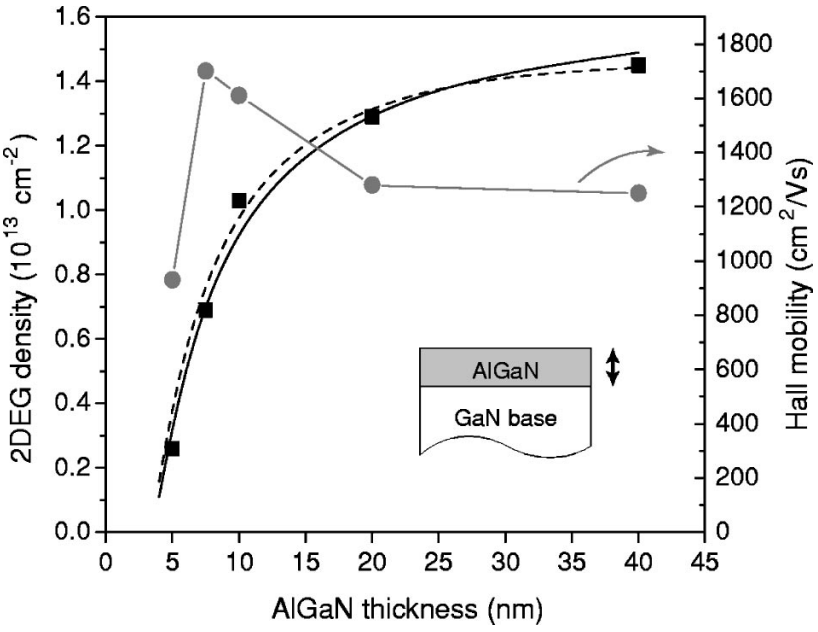



**Figure 1.2.2.2:** Effect of AlGaN thickness on carrier concentration and mobility [13]

### 1.2.3 Size and Cost

Given in equation 1.3 is the relationship between breakdown voltage and source-drain gap, which is the distance between the source and drain terminals. It can be seen that the breakdown voltage is proportion to the drift width. From the parameters given in table 1.2.1, to achieve the same breakdown voltage as that of Si, the drift region of GaN can be made 10 times smaller due to the high critical electric field, thus a reduction in the size of GaN devices can be made.

$$\mathrm{BV} = \frac{1}{2}\mathrm{W_{drift}}.\mathrm{E_{cl}}\ [10] \qquad 1.3$$

$$\mathrm{W_{drift}} = \text{source drain gap}$$

Further, growth of GaN-on-GaN epitaxy is expensive and can only be grown on small diameter substrates [14]. Therefore, the growth of GaN is carried out on foreign substrates such as silicon carbide, sapphire and silicon. By producing GaN on Si substrates, which are already available at low cost and in large diameters, the raw material cost can be kept to a minimum and a higher number of devices can be produced from each wafer reducing the cost per device.

In conclusion, due to higher efficiency along with the added benefits of the lower cost and size, devices realised using GaN could therefore outperform Si-based devices. Consequently, with the widespread (>90%) adoption of GaN-based electronics, significant energy savings in the following areas can be made [6]:

- 12% in transportation (motors in electric vehicles, trains etc)
- 20% in consumer electronics
- 8% in lighting (in combination with GaN LEDs)
- 20% in IT infrastructure (power distribution in server farms etc)

## 1.3 Key Challenges

Despite the superior material qualities of GaN, certain issues need to be addressed before these technologies replace Si-based devices. Due to the existence of the 2DEG when an AlGaN is grown on GaN, the devices are always in the ON state. Therefore, for fail-safe operation normally-off type devices in which no current flows at 0V gate bias is strongly required [11]. This can be achieved by recess etching the gate region of the AlGaN to make sure the AlGaN barrier is not thick enough to induce the 2DEG. This could also be achieved by the growth of a thinner AlGaN barrier, however control of such small thicknesses during growth is difficult. Another approach is fluorine implanting the AlGaN with the use of a fluorine-based plasma pretreatment. The fluorine ions provide the threshold voltage shift necessary for normally-off operations [1]. An alternative method includes a cascode type devices using a silicon transistor in series with a normally-off GaN transistor.

In addition, the presence of leakage paths indicated in Figure 1.3.1 can reduce the efficiency and reduce the maximum breakdown voltage of the device. The leakage paths are discussed in detail below:

- Due to the large lattice and thermal coefficient mismatch between Si and GaN, the buffer region needs to be carefully engineered. Defects in the buffer region can give rise to high leakage currents that would result in device degradation and hinder the device from reaching its maximum breakdown voltage [15]. Doping the buffer region with either iron or carbon atoms has been used to mitigate this [16].

- Surface leakage between the gate and drain results as a consequence of defects, which compensate the surface donors that are necessary for the generation of the 2DEG. This can reduce the maximum drain current and also result in higher $R_{ON}$ [17]. Passivation of these defects by using insulators such as silicon nitride ($SiN_x$) can help reduce the surface leakage [17, 18].

- Gate leakage is a parasitic conduction path that occurs as a consequence of defects on the GaN surface. It can lead to reduced efficiency of the device and result in lower breakdown voltages [18]. Lower off-state currents are also necessary for normally-off operations and to make sure the static power consumption is minimised [14]. Gate leakage can be minimised by the incorporation of an insulator between the gate metal and the semiconductor. However, the introduction of an insulator-semiconductor interface can also increase leakage if the interface and the oxide aren't defect free. Therefore, in addition to depositing an insulator, optimised insulators and pretreatments prior to the oxide deposition and post treatments help decrease gate leakage.

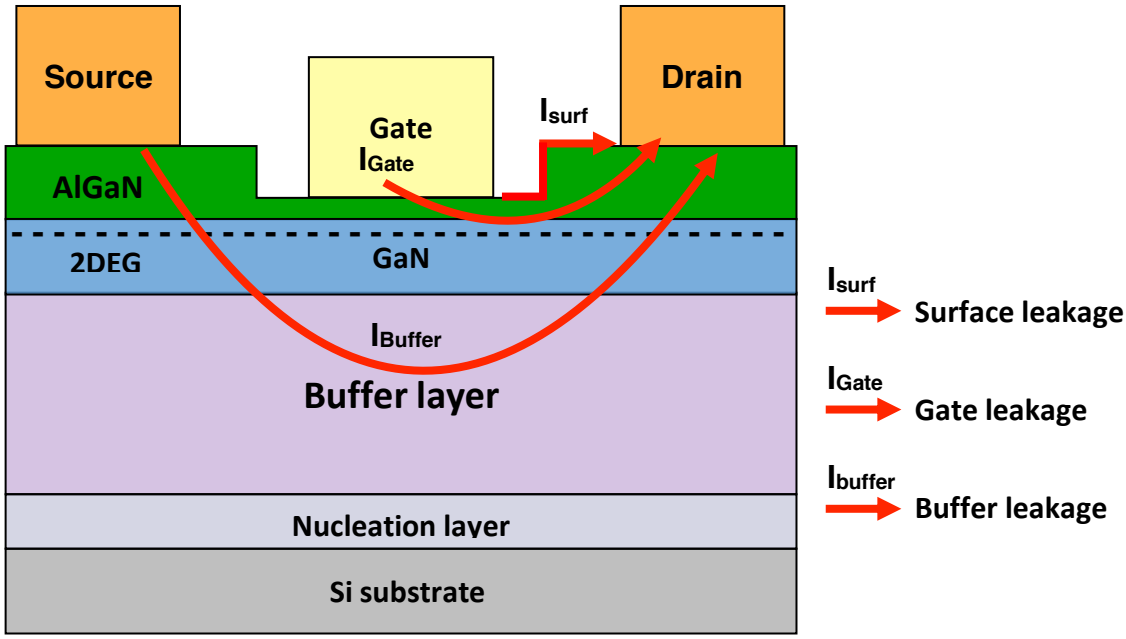



**Figure 1.3.1:** Leakage paths of AlGaN/GaN HEMT

## 1.4 Scope and outline of this thesis

This thesis focuses on optimising the gate region of GaN devices. It has been reported that the surface contamination of GaN surfaces consist of oxygen, carbon and adsorbates from the atmosphere. Therefore, this work explores processing of a GaN surface that avoids air exposure. This has been achieved by using GaN samples that have an in-situ grown $SiN_x$ cap on top of the GaN as part of the wafer growth. A clustered plasma etch and atomic later deposition tool has been utilised to etch the $SiN_x$ and transferred under vacuum ($10^{-9}$ Torr) to the ALD chamber where various plasma pretreatments and dielectric and metal depositions have been performed. The details of the operation of this equipment are given in chapter 4.

To reduce the gate leakage the impact of atomic layer deposited (ALD) dielectrics on GaN has been investigated. The dielectrics used in this work were aluminium nitride (AlN) and aluminium oxide ($Al_2O_3$). AlN has been used as an interlayer between GaN and $Al_2O_3$ because it has been proven to reduce the stress between the GaN and $Al_2O_3$ [19]. However, imperfections at the dielectric-GaN interface can lead to the creation of defects in the band gap that serves as interface states that can reduce the density of carriers by trapping electrons [20] [21]. Further fixed charges in the dielectric itself and interface states can result in reducing the mobility of carriers due to coulomb scattering [20] [22]. Therefore, to ensure creation of a low defect dielectric-GaN interface various plasma pre-treatments have also been explored. To ensure low charge density in the dielectric, the effect on the electrical properties of a forming gas anneal (FGA) after aluminium oxide deposition was also examined. Furthermore, the effect of an in-situ atomic layer deposited gate was also investigated. The impact of these were measured electrically using metal oxide semiconductor capacitors (MOS capacitors).

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**The organisation and contents of this Thesis are as follows:**

Chapter 2 provides the background needed for understanding atomic layer deposition (ALD), chapter 3 provides the theoretical background needed for understanding MOS capacitors, chapter 4 details the fabrication and equipment used for MOS capacitor

production, chapter 5 explains how the MOS capacitors in this work are characterised , chapter 6 outlines the effects of an "in-situ" processed GaN surface that is never exposed to the atmosphere, chapter 7 outlines the effect of an AlN interlayer between GaN and $Al_2O_3$, chapter 8 outlines the effects of incorporating a TiN gate metallisation and finally chapter 9 discusses conclusions and future work.

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# 2. Atomic Layer Deposition (ALD)

## 2.1 Introduction

This chapter gives an overview of the fundamentals of atomic layer deposition (ALD). The chapter begins by describing the importance of ALD and how an ALD cycle operates. This is followed by a description of the ALD growth windows and different growth rates that can result during ALD. The chapter concludes with a description of ALD reactors in general use and in particular, the way they can be configured for plasma based ALD.

## 2.2 Background

Thin and conformal dielectric and metal films have become an essential part of contemporary solid-state electronic devices. These include transistors, solar cells, micro-electromechanical systems (MEMS) and other emerging technologies [1]**.** To date physical vapour deposition (PVD) and chemical vapour deposition (CVD) have been the most widely used film deposition techniques [2]. PVD are deposition techniques where the film in its vapourised form condenses on to the required sample, the substrate. The vapourised form is usually obtained either thermally, induced by a laser or through sputtering by energetic ion bombardments. In CVD, films are grown by chemical reactions to reactants that are supplied simultaneously into a chamber [3]. The reactions are either thermally driven by heating the substrate or are activated by reactive species in a plasma. However due to the continuous trend in downsizing of devices and processing devices on large substrates (6" wafers) PVD and CVD are reaching the limits in delivering these demands. Due to the requirements in current technology the recent interest in film growth requires precise thickness control, high uniformity on wafers and conformity on high aspect ratio patterns, making alternative deposition techniques such as atomic layer deposition (ALD) most favourable [2].

ALD is a vapour phase deposition technique that is used to grow thin films [4]. In contrast to the formerly detailed deposition techniques, ALD is a self-limiting sequential growth process where the reactants are exposed to the substrate in separate stages. The reactants consist of a precursor and a reactive gas often referred to as a co-reactant. Precursors are

either organic compounds or halides consisting of a metal atom and a ligand [5]. The individual exposure of the reactants to the substrate ensures that no cross-reactions between reactants occur, resulting in films with very high purities.

ALD was first researched in 1960s by Russian scientists and was later patented in 1970s by Finnish researcher Suntola [6]. Today ALD has been adopted in many different technologies; in metal-oxide-semiconductor field effect transistors (MOSFETs), solid oxide fuel cells (SOFC), solar cells and many more [7]. It is used to grow insulators such as hafnia, alumina and aluminium nitride as well as metals including titanium nitride, platinum, palladium and tantalum [7]. Due to its cyclical and self-saturating nature, ALD can achieve films with precise thicknesses. Further its parameters such as precursor and co-reactant exposure times can be adjusted to increase uniformity and conformity on high aspect ratio structures. In addition, the reactant gas ratios can also be altered to tune film compositions **[2].**

An ALD cycle can be divided in to two half-reactions, also known as half cycles as illustrated in Figure 2.2.1:

**1(a).** First, the substrate is exposed to a precursor that becomes chemically bonded to the surface (chemisorption). Chemisorption is brought about by either a ligand exchange mechanism, dissociation or association [5].

Ligand exchange mechanism as indicated in Figure 2.2.2(a) occurs when part of a molecule is exchanged with a chemical group at the surface of the substrate. Dissociation on the other hand, takes place when part of a molecule can split into smaller fractions and part or all of the molecule is adsorbed on to the substrate as shown on Figure 2.2.2(b). In contrast as depicted on fig. 2.2.2(c) association occurs when the complete molecule chemisorbs on to the substrate. Once the surface is covered with a monolayer of the precursor, no more reactive sites are offered to the same precursor and hence no further reactions occur.

However, chemisorption can be limited by steric hindrance; where a precursor molecule after being adsorbed by some reactive sites, is large enough that it blocks access to other reactive sites. Chemisorption can also be limited if the precursor is adsorbed only to specific reactive sites of a surface. The nature of the reactive sites and the surface density depends on the material, its crystal orientation and surface pretreatments [5].

**1(b)** Following the exposure of the reactants**,** unreacted precursors and byproducts are then purged from the chamber using an inert gas, usually nitrogen or argon. This ensures that no cross-reactions between the co-reactant and the precursors occur.

**2(a)** The substrate is then exposed to the co-reactant, a reactive gas that reacts with the chemisorbed precursor

**2(b)** Finally excess reactive gas and byproducts are purged from the chamber using an inert gas such as nitrogen or argon.

This cycle repeats until the required thickness is deposited.

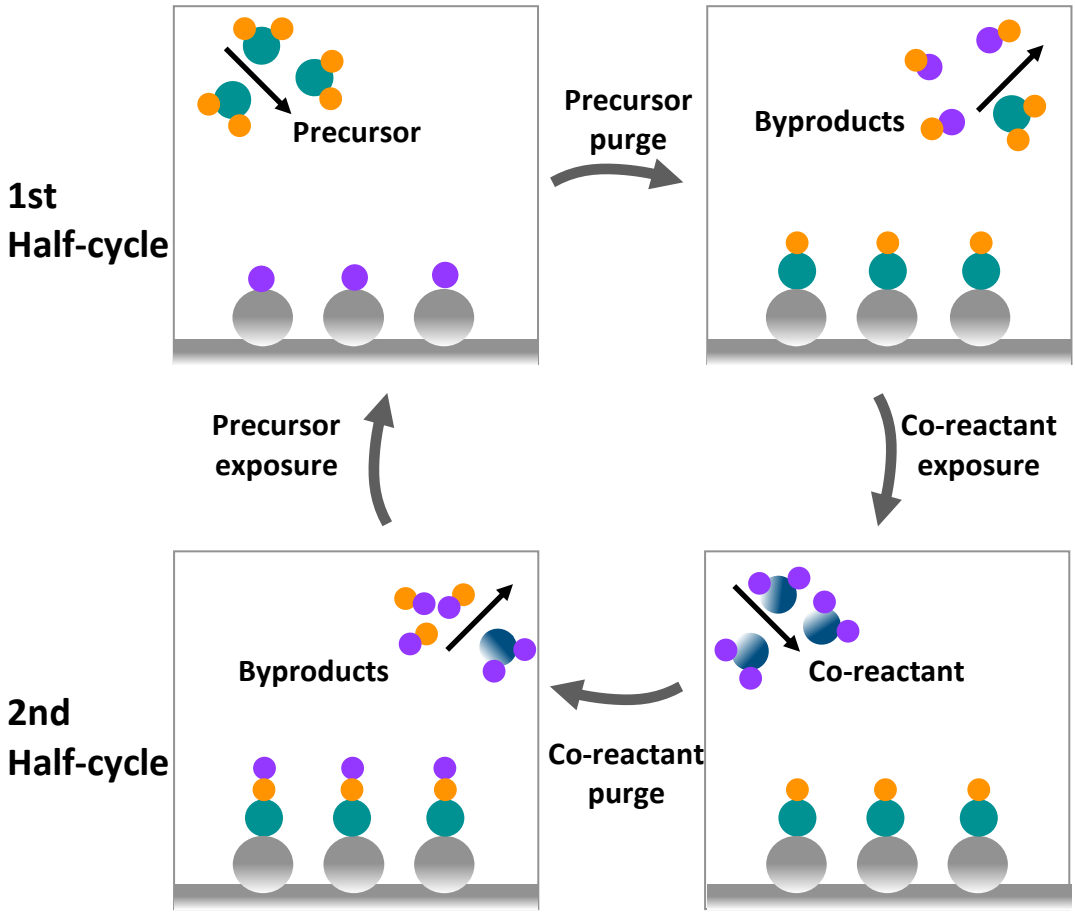


**Figure 2.2.1: An ALD cycle**

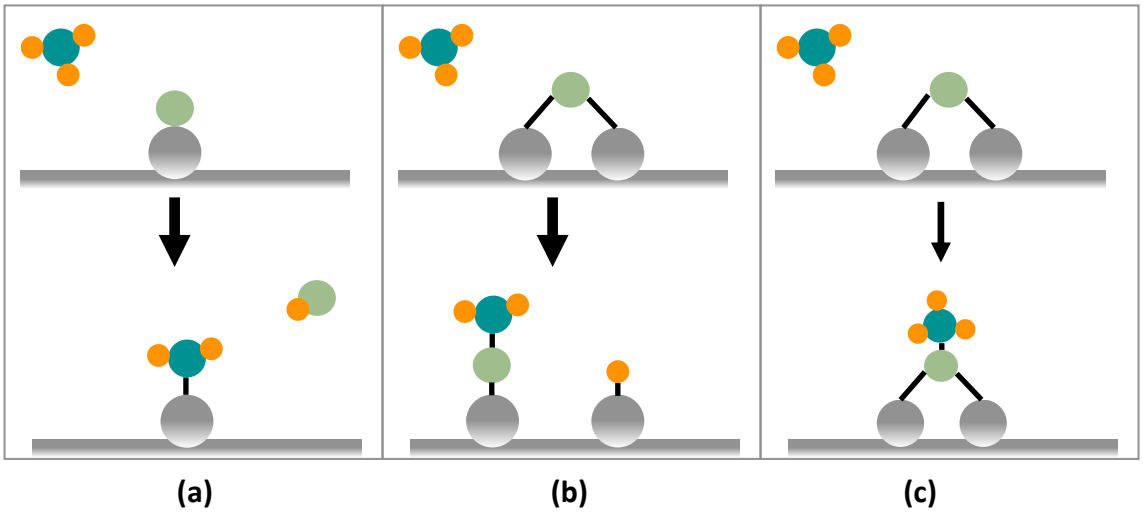


**Figure 2.2.2: Chemisorption mechanisms (a)Ligand exchange (b)Dissociation (c)Association**

An ALD reaction can take place either by the assistance of a plasma or thermally. In plasma assisted ALD, during the reactant step the samples are exposed to reactive species generated by a plasma. In Thermal ALD the surface reactions take place at elevated temperature without the presence of a plasma [3].

## 2.3 ALD window

Each ALD process consists of an optimum region for film growth. The main factors affecting this are temperature, precursor and co-reactant dose time and their purge times.

### 2.3.1 ALD temperature window

For an ideal ALD growth, the temperature window is the temperature range at which the growth per cycle (GPC) remains unaffected to any changes in the temperature. As shown in Figure 2.3.1, it is the region at which GPC remains constant. Temperatures below the ALD window range result in non-ALD type films either due to slow kinetics or due to CVD type reactions caused by condensation of precursors on the substrate. Temperatures above can either cause desorption of precursor molecules from the substrate resulting in slower GPC or decomposition of precursors giving rise to CVD type reactions.

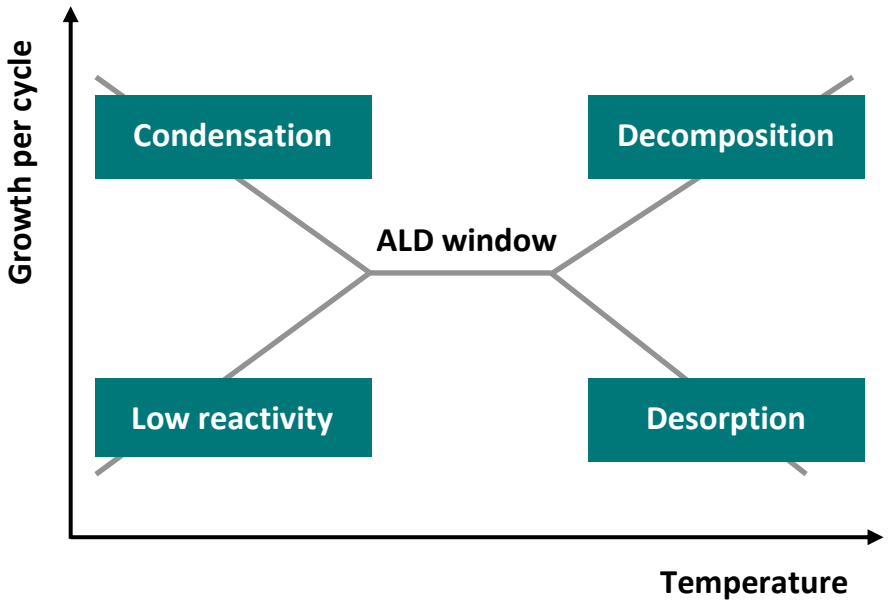


**Figure 2.3.1: ALD Temperature window**

### 2.3.2 Precursor exposure time and purge times

It is necessary to make sure that the dose time is sufficiently long to give enough time for the whole substrate surface to be covered (coverage). Sufficient time should also be given to make sure that all the reactants are purged out, so CVD type reactions don't occur as shown on the graphs in Figure 2.3.1.

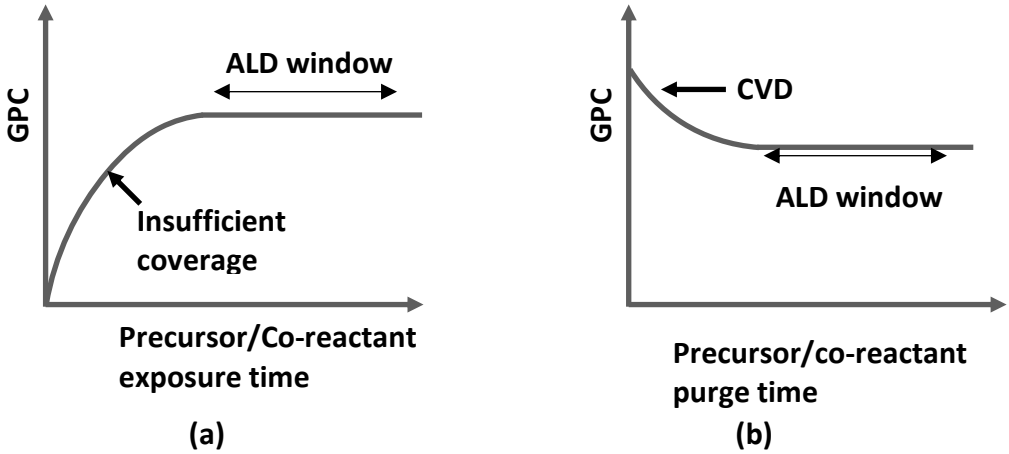


**Figure 2.3.2: (a)ALD Precursor/co-reactant exposure window and (b)ALD precursor/co-reactant purge window**

## 2.4. Growth rate

An ideal growth rate in an ALD process should be constant and independent of the number of cycles. However, the growth rate isn't always constant, and it is dependent on the substrate used and the different pretreatments performed [2]. The different ALD nucleation behaviours which give rise to different growth rates are shown in Figure 2.4.1. A higher density of reactive sites on the substrate compared to the ALD film result in the initial growth rate being higher giving rise to a surface enhanced growth [5]. On the contrary, a nucleation delay can occur if reactive sites on the surface are lower than on the film giving rise to a type 1 surface inhibited growth [5]. It is also possible for ALD to start at a limited number of nucleation sites resulting in rough growth islands, thus resulting in an increased initial growth rate. However, as these islands start to coalesce the roughness in the films decreases, reducing also the GPC of the film, as shown in Figure 2.4.1. This type of growth rate is known as type 2 surface inhibited growth [5].

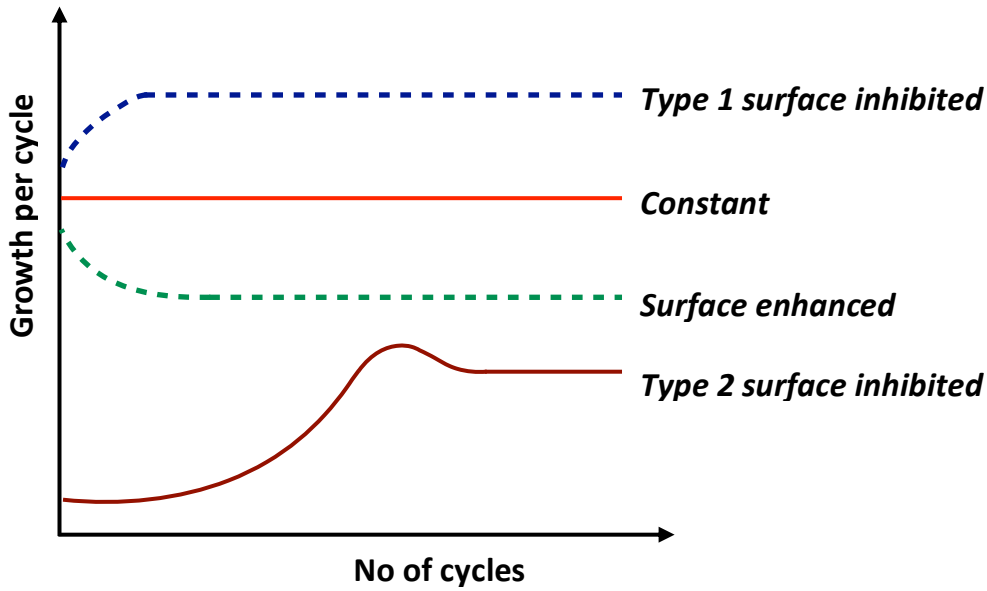


**Figure 2.4.1: ALD growth per cycle vs no. of cycles for different ALD nucleation behaviours**

## 2.5. ALD reactors and plasma configurations

### 2.5.1 ALD reactors

Due to the cyclical nature of ALD where precursors and co-reactants need to be pumped in and purged out regularly, the reactors need to be built in such a way that they are able to

constantly pulse reactants in and out. The architecture of different ALD reactors are portrayed in Figure. 2.5.1 These include:

- Flow-type ALD [3]: The reactants enter the reactor on one side as shown in Figure 2.5.1(a) and leave on the opposite side. However, since the volume of the reactor is very low, reactants tend to undergo many collisions producing lower concentrations of reactants at the other end of the reactor. This can result in non-uniform films.
- Showerhead ALD [3]: In this type of reactor the reactants are introduced though a showerhead in to the chamber. This ensures even distribution of the reactants.
- Spatial ALD [3]: This uses different zones to expose and purge precursors and co-reactants, therefore the substrate itself needs to be moved from one zone to another.
- Batch ALD [3]: Batch ALD reactors are used when high throughput is essential. These reactors can house several wafers onto which materials can be deposited at the same time. However due to the large reactor volumes, the time needed to expose precursors and co-reactants would need to be increased.

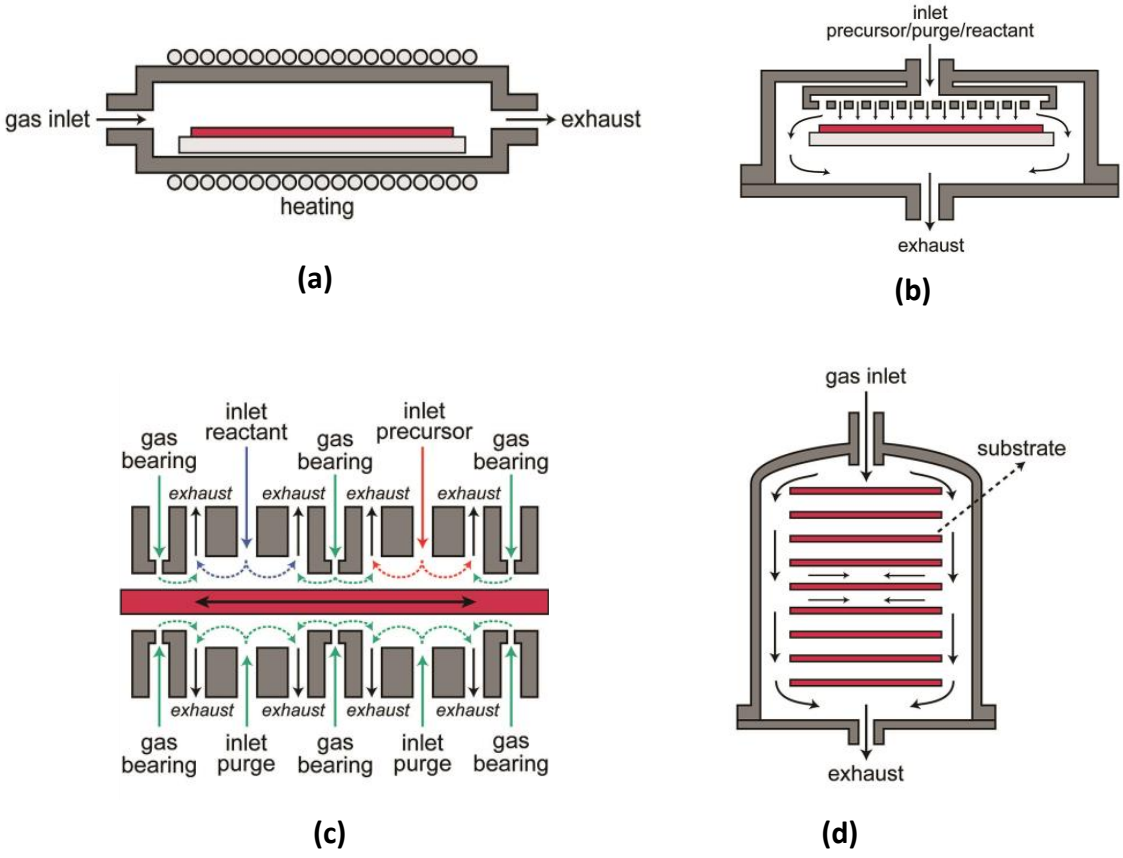


**Figure 2.5.1: ALD reactors (a) Flow-type ALD, (b) Showerhead ALD, (c) Spatial ALD, (d) Batch ALD [3]**

### 2.5.2 Plasma configurations

The three most popular plasma sources are direct, remote and radically-enhanced plasma illustrated in Figure 2.5.2. The operation of these will be discussed in detailed below.

**Direct plasma**

As shown in Figure 2.5.2(a) the plasma is generated between two electrodes and the wafer is positioned at an electrode directly beneath the plasma, which is grounded. Direct plasma configurations can produce films with very high uniformity. However, it can also cause high damage due to the interaction of energetic ions with the substrate

**Remote plasma**

As the name suggests, in this configuration (shown in Figure 2.5.2(b)) the plasma source is located remotely from the substrate stage. As opposed to the direct plasma configuration, the substrate is not involved in the generation of the plasma and can therefore produce a plasma that is less damaging.

**Radically-enhanced plasma**

In the third configuration (shown in Figure. 2.5.2(c)) the plasma source is situated away from the substrate and the generated plasma speciesare required to flow through a tube between the chamber and the plasma source before reaching the substrate. There the plasma undergoes many collisions losing its electrons and ions before reaching the substrate. Hence referred to as radically-enhanced plasma.

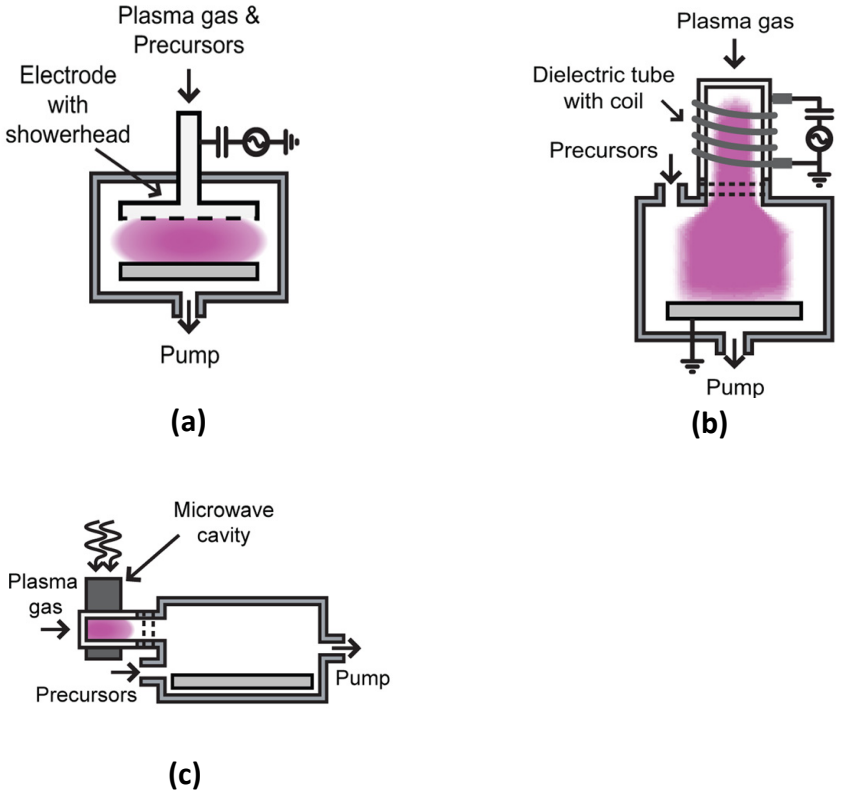


**Figure 2.5.2: Plasma sources: (a) Direct plasma, (b) Remote plasma and (c) Radically-enhanced plasma [4]**

## 2.6 Summary

This chapter explains the operation of an ALD cycle, the different ALD windows that are needed to be identified and the different ALD reactors and the plasma configurations that exist. Information is also given on the different growth rates that can occur during an ALD process.

## 2.7 Reference

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# 3. Metal-oxide-semiconductor capacitor (MOS capacitor)

## 3.1 Introduction

This chapter gives an overview of the theory and operation of metal –oxide-semiconductor (MOS) capacitors. The chapter begins by describing characteristics of ideal MOS capacitors and their electrostatics at different biasing regimes. It then explains the capacitance-voltage (C-V) response of ideal MOS capacitors and describes how C-V measurements are performed. Finally, non-idealities are described along with their effect on C-V response.

## 3.2 Background

An MOS capacitor is a two terminal device consisting of an oxide sandwiched between a metal and a semiconductor as illustrated in Figure 3.2.1. The two terminals consist of a contact at the top of the oxide; the gate, and a contact made to the semiconductor; the ohmic contact. The capacitance-voltage characteristics of an MOS capacitor can be used to ascertain useful information regarding the quality of, and any non-idealities in the oxide, the oxide-semiconductor interface and also the oxide-gate metal interface. CV characteristics are in essence a window representing the nature of the internal structure of MOS capacitors [1].

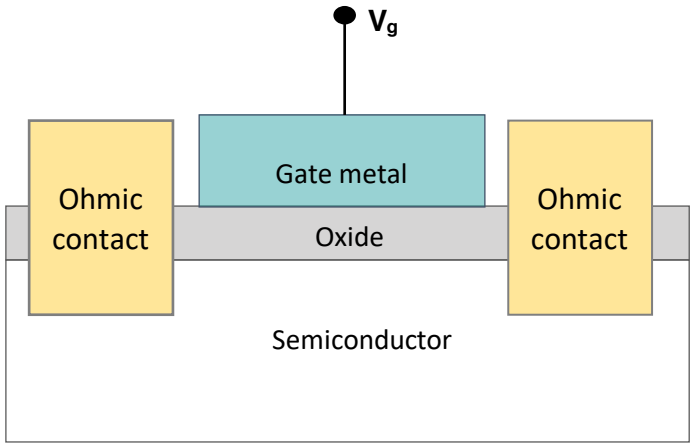



**Figure 3.2.1: Cross section of a MOSCAP**

The following section describes electrostatic properties of an ideal MOS capacitor, where the majority carriers are electrons, also known as an n type MOS capacitor or an n-MOS capacitor. Energy band diagrams are used as an aid to understand C-V properties at equilibrium (zero bias) and at different biasing regimes; notably accumulation, depletion and inversion.

**Characteristics of an ideal MOS-capacitor**

An ideal MOS capacitor has the following properties:

- The oxide is a perfect insulator and has zero current flowing through it under all biasing conditions.
- There is no charge or defects present in the oxide, at its surface or at the semiconductor-oxide interface.
- For any biasing conditions, the only charge present is that in the semiconductor and that of equal but opposite polarity at the metal/dielectric interface.
- The work function difference between the metal, $\Phi_m$ and the semiconductor, $\Phi_s$ is zero, ($\Phi_{ms} = \Phi_m - \Phi_s = 0$).

# 3.3 Electrostatics of an MOS-capacitor

Figure 3.3.1 illustrates the band diagram of an ideal n-MOS capacitor in equilibrium. The work functions, $\Phi_m$ and $\Phi_s$ represent the energy required to remove an electron to the vacuum level from the metal and semiconductor respectively. To proceed further with the explanation of MOS band diagrams, it is important that a few parameters be defined. These include the surface potential $\phi_S$, and bulk potential, $\phi_B$, and the band bending, $\psi_S$. To describe these, firstly, the potential at any point in the semiconductor $q\phi_s(x)$ is determined in equation 3.1, where x is the distance from the dielectric-semiconductor interface to the bulk of the semiconductor. $\phi_S$ therefore, is the potential at which x=0 and $\phi_B$ is the potential when x tends to infinity, as shown in Equations 3.1 to 3.4. $\psi_S$ is the difference between the surface and bulk potentials (equation 3.5). These parameters are presented in Figure 3.3.1(a) and (b) and will be used when describing band diagrams. Figure 3.3.1(b) is a result of an application of a positive bias, $V_g$, with bands bending in the downward direction, i.e. $\psi_S > 0$.

In a MOS system with zero work function difference between metal and semiconductor, the band diagram shown in Figure 3.3.1(a) is achieved. This stage where $\phi_s = \phi_B$ and band

bending is equal to zero, is also known as the flat band region and occurs when the applied bias is zero. During the application of a bias, the metal and semiconductor Fermi levels move such that the energy between them amount to equation 1.6. This is brought forward by the movement of charge to and from the oxide-semiconductor interface. Electric fields are then established in the oxide by surface charge layers that are formed in the metal and oxide.

$q\phi(x) = E_{FS} - E_i(x)$ [2] 3.1

When, $x = 0,\ \phi(0) = \phi_S = \text{surface potential}$ 3.2

When $x \to \infty,\ \phi(x \to \infty) = \phi_B = \text{bulk potential}$ 3.3

$\psi(x) = \phi(x) - \phi_B$ = band bending at a point [2] 3.4

$\psi_S = \phi_S - \phi_B$ = total band bending 3.5

$E_{f(metal)} - E_{f(semiconductor)} = -qV_g$ [1] 3.6

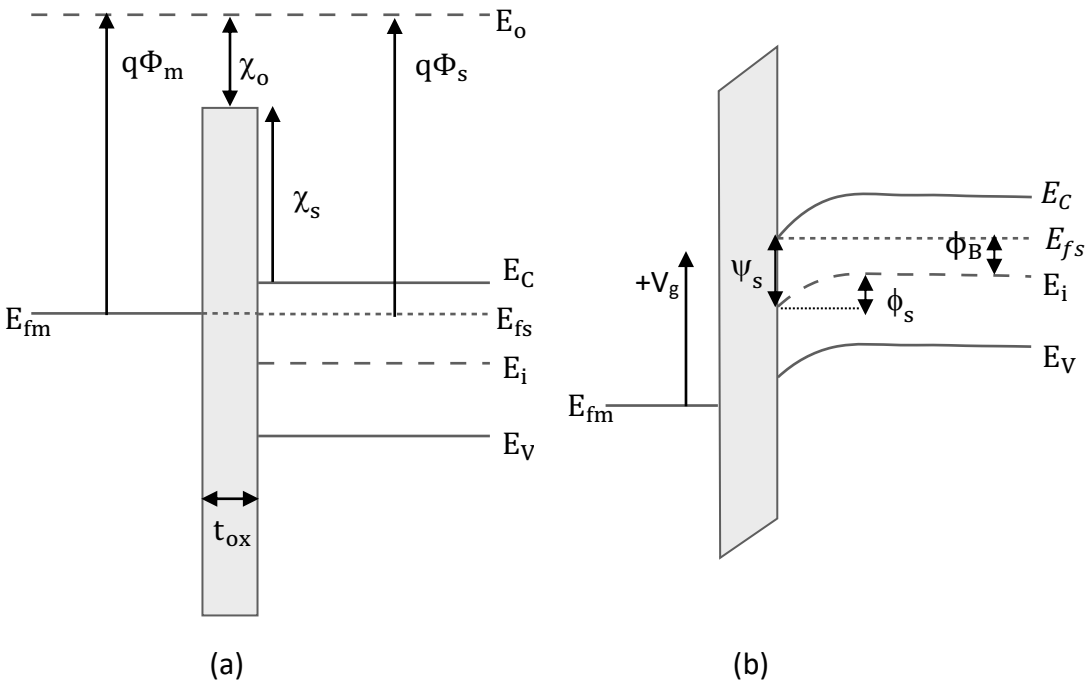



**Figure 3.3.1: (a) Band diagram under flat band condition and (b) band diagram under applied bias. Where, $E_c$ is the conduction band maximum, $E_{fm}$ is the Fermi level of the metal, $E_{fs}$ is the Fermi level of the semiconductor, $E_i$ is the intrinsic level and $E_0$ is the vacuum level**

### 3.3.1 Accumulation

The application of a positive gate voltage ($V_g$>0), places positive charge on the gate electrode. To maintain charge neutrality, negatively charged electrons are drawn towards the oxide-semiconductor interface. This causes a band bending in the downward direction at the oxide-semiconductor interface, hence $\psi_S$ and $\phi_S$ are both greater than zero. In this particular instance, where the majority carrier concentration near the oxide-semiconductor interface is higher than in the bulk, is known as accumulation. The charge carrier concentration at the oxide-semiconductor interface is given by equation 3.7. Figure 3.3.2 (a) shows the band bending along with the block charge diagram in accumulation. Block charge diagrams show the charge distribution at different bias voltages. It doesn't represent the exact charge distribution, instead it is qualitative in nature, giving an indication of the magnitude and the spatial extent of the charge.

$$n_s = n_i \exp\left(\frac{q}{KT}\psi_s\right) \quad 3.7$$

$n_i = \text{intrinsic carrier concentraion}$

$$n_i = \sqrt{N_C N_V}\exp\left[-\frac{(E_C - E_V)}{2kT}\right] \quad 3.8$$

$N_C = \text{Densitiy of states in the conduction band}$

$N_V = \text{Density of states in the valence band}$

### 3.3.2 Depletion

The application of a small negative gate voltage ($V_g$<0), places a negative charge on the gate, repelling electrons from the oxide-semiconductor interface and exposing the positively charged donors. In other words, the electrons are depleted away from the surface. This is represented by the bands bending in the upward direction and $\psi_S$ and $\phi_S$ are both less than zero. This situation where the electron concentration at the surface is less than that of the donor concentration is known as depletion. As the bias voltage is made more negative, the depletion layer widens ultimately reaching a maximum depletion width shown in equation 3.9.

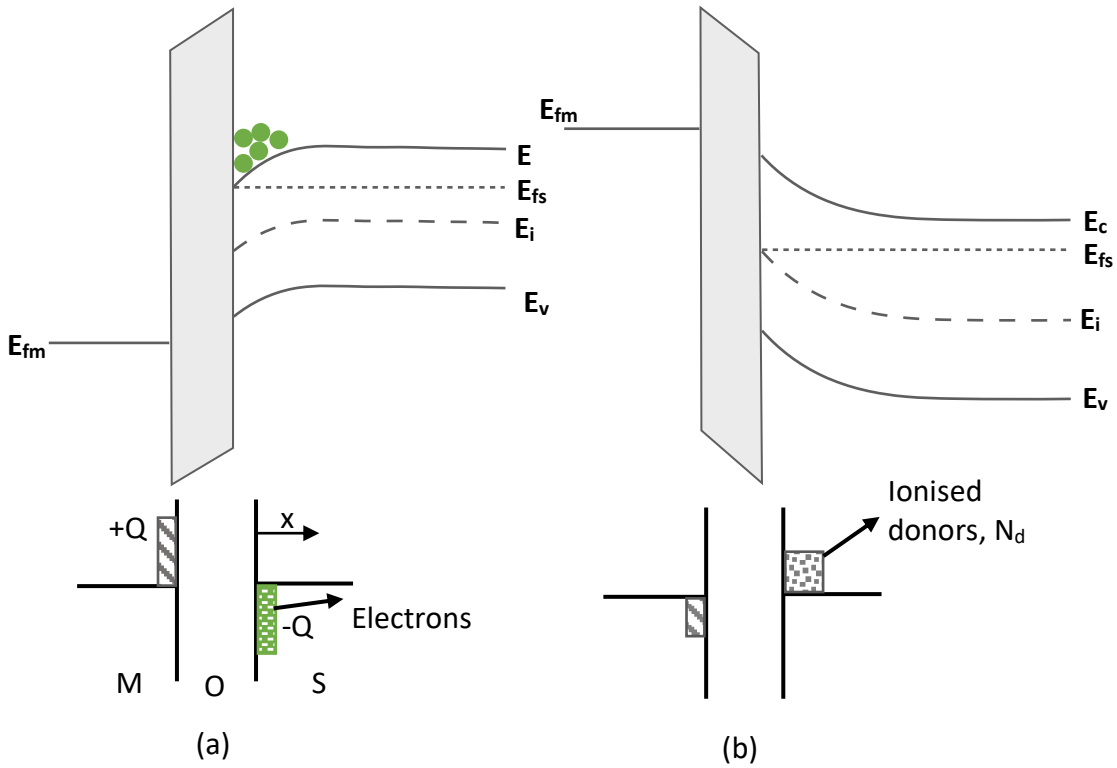
$$\text{Depletion width} = \sqrt{\frac{2\varepsilon_o \varepsilon_S \psi_S}{qN_A}} \quad 3.9$$

### 3.3.3 Inversion

Decreasing the gate voltage even further attracts minority carriers to the surface. The voltage at which the minority carriers start to appear at the surface is known as the threshold voltage, $V_T$, which occurs when $\psi_S=2\phi_B$ given in equation 3.10 [1]. This is shown in Figure 3.3.2(c). As the bias voltage is decreased further the minority carrier concentration at the surface increases more than the bulk majority carriers and the nature of the surface inverts from an n-type to that of a p-type. This is indicated in Figure 3.3.2(d).

$$\psi_{s,Threshold} = 2\phi_B = \frac{-2kT}{q}\ln\left(\frac{N_D}{n_i}\right) \qquad 3.10$$

Table 3.3.1 summarizes, the operating regions along with their corresponding surface potentials and carrier densities.



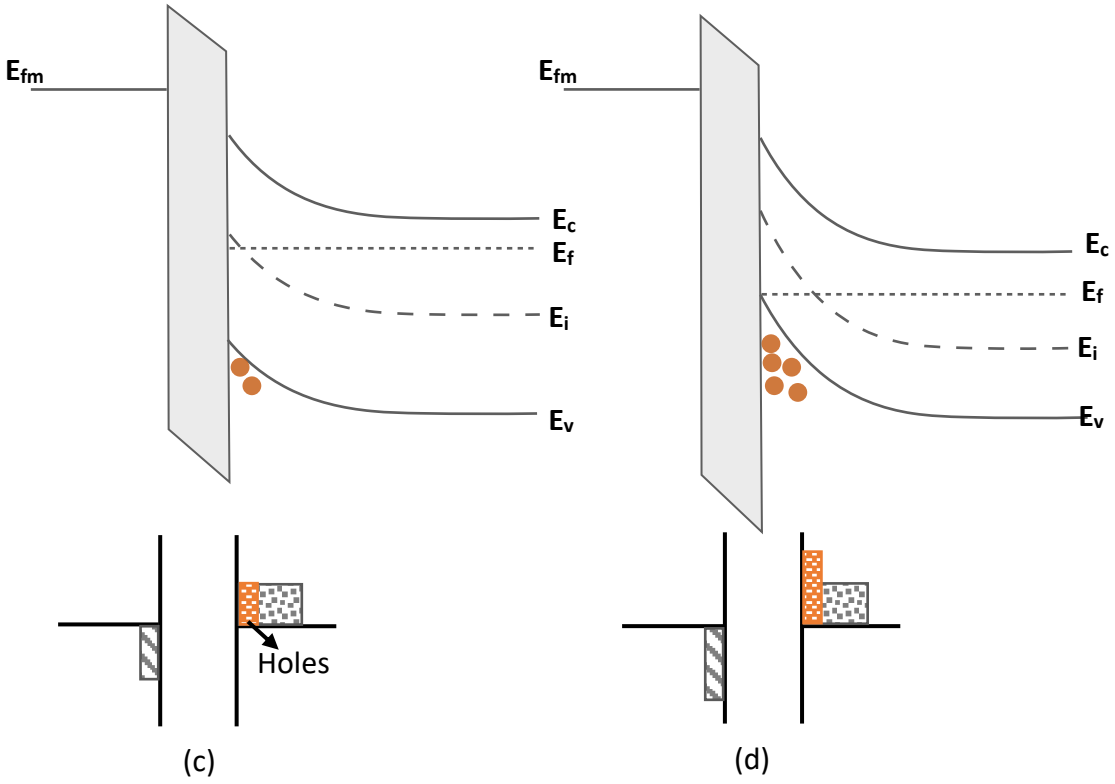



**Figure 3.3.2: Band and block charge diagram of an n-MOS capacitor under (a)accumulation, (b) depletion, (c) threshold voltage and (d) Inversion**

| Operating region | Surface Potential/eV | Surface Carrier density/$cm^{-3}$ |
|---|---|---|
| Flat band | $\psi_S = 0$ | 0 |
| Accumulation | $\psi_S > 0$ | $n_s > N_d$ |
| Depletion | $\psi_S < \phi_B < 0$ | $N_d$ |
| Threshold | $\psi_S = 2\phi_B$ | $p_s < N_d$ |
| Inversion | $\psi_S > 2\phi_B < 0$ | $p_s > N_d$ |

**Table 3.3.1: Summary of operating conditions of an n-MOS capacitor**

The next section describes how MOS capacitors are measured and examines the C-V properties at the relevant biasing regions.

# 3.4. C-V curve of an ideal MOS-capacitor

The equivalent circuit of an ideal MOS capacitor is shown in Figure 3.4.1, the total capacitance is the sum of the oxide, $C_{ox}$ and the semiconductor capacitance, $C_s$. The semiconductor is indicated as a variable capacitor since it is bias dependent and changes as a function of band bending at the interface.

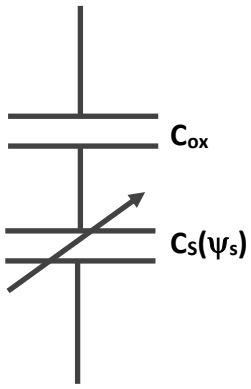
In order to perform C-V measurements, two voltage sources are applied simultaneously to the device under test, $C_{DUT}$. The two sources include a small AC signal (~20mV) and a DC voltage that is swept in time. The DC voltage provides the bias necessary to sweep the C-V curve from accumulation to inversion (and vice versa) and the AC voltage provides the voltage required for measuring the capacitance at a point in time. The capacitance of the device is calculated by the division of the measured current by the voltage as indicated in equation 3.11 [3].

$$C_{DUT} = \frac{I_{DUT}}{2\pi f V_{AC}} \text{ [3]} \qquad 3.11$$

$C_{DUT} =$ Capacitance of the device under test,

$I_{DUT} =$ Magnitude of AC current through the device, $f =$ test frequency,

$V_{AC} =$ Magnitude and phase angle of the measured AC voltage




$C_{ox}$= oxide capacitance

$C_s$ = Semiconductor capacitance

**Figure 3.4.1: Equivalent circuit of a MOSCAP**

Further, to obtain C-V data, the majority and minority carriers need to be able to respond to the applied AC signal. In other words, accumulation and depletion arise as a result of majority carriers moving to and from the depletion layer. The majority carriers will respond to the ac voltage so long as the period of the AC signal is greater than the majority carrier

response time ($\tau_{maj}>1/\omega$), also given by equation 3.12. This frequency usually occurs at 1MHz or less [1]. Inversion on the other hand is achieved due to minority carriers and hence are dependent on the minority carrier response time ($\tau_{min}>1/\omega$) defined in equation 3.14. Therefore, the measurement of C-V is dependent on the frequency of the signal applied.

$$\text{Majority carrier response time} = \tau_{maj} = \frac{\lambda^2}{\mu\frac{kT}{q}} \text{ [2]} \qquad 3.12$$

Where, $\lambda$ is the Debye length

$$\lambda = \sqrt{\frac{kT\varepsilon_s}{q^2 n}} \qquad 3.13$$

$\varepsilon_s = \text{Permitivity of semiconductor}$

$\mu = \text{carrier mobility}$

$$\text{Minority carrier response time} = \tau_{min} = \frac{1}{\sqrt{2}}\frac{N_D}{n_i}\tau_T\sqrt{\left(1-\frac{\psi_T}{\phi_B}\right)} \text{ [2]} \qquad 3.14$$

$\tau_T = \sqrt{\tau_n \tau_p}$

$\tau_n = \text{Bulk electron life time}, \tau_p = \text{Bulk hole life time}$

Figure 3.4.1 illustrates the C-V curves that result from high and low frequency measurements at different bias voltages along with their corresponding capacitor combinations. High frequency here refers to the frequency where the period of the signal is less than the minority carrier response time. The following section describes the C-V characteristic of the different regions.

### 3.4.1 Accumulation

In an ideal MOS capacitor, under accumulation conditions, only majority carriers are involved in either adding or subtracting charge at the oxide-semiconductor surface. Therefore, the charge configuration simplifies to that of a parallel plate capacitor and is given by equation 3.15.

$$C_{acc} = C_{ox} = \frac{\varepsilon_o \varepsilon_{ox} A}{t_{ox}} \qquad 3.15$$

$C_{acc} = \text{Accumulation capacitance}, C_{ox} = \text{Oxide capacitance}$

$\varepsilon_o = \text{permivity of free space } \varepsilon_{ox} = \text{relative permittiy of oxide},$

$t_{ox} = \text{thickness of oxide}, A = \text{Area of the gate}$

### 3.4.2 Depletion

During depletion, the capacitance is similar to that of two parallel plate capacitors; the oxide and semiconductor capacitance, in series as shown in Figure 3.4.1. The total capacitance amounts to that shown in equations 3.16.

$$C_{dep} = \frac{C_{ox}C_s(\psi_s)}{C_{ox}+C_s} \quad 3.16$$

$$C_S = \frac{\varepsilon_o\varepsilon_s A}{W_D(\psi_s)} \quad 3.17$$

$$W_D(\psi_s) = \frac{2\varepsilon_s\varepsilon_0}{qN_D}\psi_s \quad 3.18$$

$C_S =$ Semiconductor capacitance, $\varepsilon_s =$ permitiy of semiconductor, $W_D =$ Depletion width,

### 4.3 Inversion

During inversion, the C-V curve can follow two paths. If the time period of the applied AC signal is greater than the minority carrier response time, capacitance is that of a parallel plate capacitor as shown in equation 3.19. This is shown by the solid line in figure 3.4.1. Alternatively, if the period of the AC signal is lower than the minority carrier response time, during inversion the C-V curve reaches a constant capacitance at the maximum depletion width, given by equation 3.21. The total capacitance is then the series combination of the oxide and semiconductor capacitance with the maximum depletion width.

$$C_{inv} = C_{ox} \quad \text{if} \quad \frac{1}{\omega} > \tau_{min} \quad 3.19$$

$$C_{inv} = \frac{C_{ox}C_s}{C_{ox}+C_s} = \frac{C_{ox}}{1+\frac{\varepsilon_o W_{Dmax}}{\varepsilon_s t_{ox}}} \quad 3.20$$

$$\text{Maximum depletion width} = W_{Dmax} = \sqrt{\frac{2\varepsilon_o\varepsilon_s}{qN_D}(2\phi_B)} \quad 3.21$$

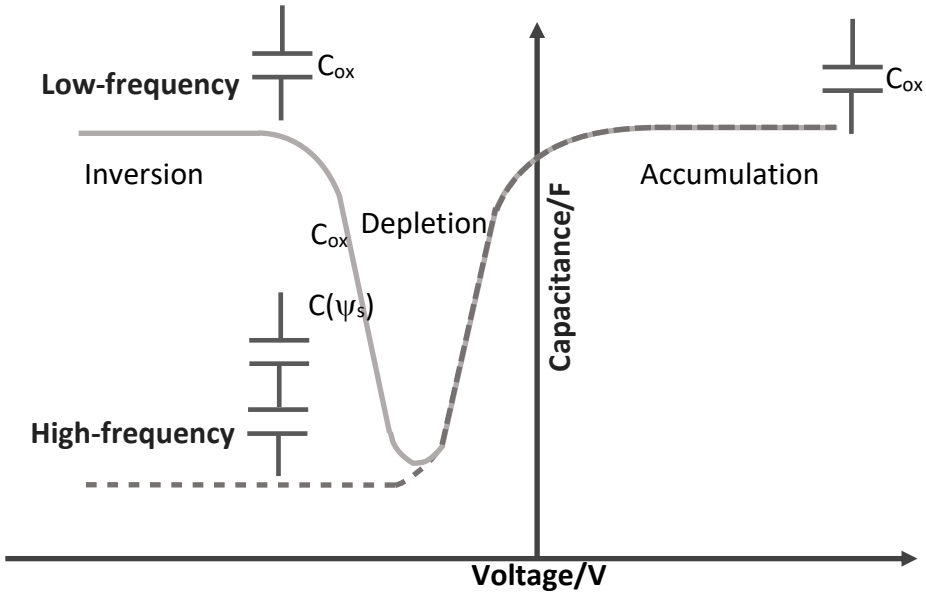



**Figure 3.4.1: C-V characteristics of an ideal MOS capacitor at high and low frequency**

## 3.5. Non-idealities of an MOS-capacitor

Although the ideal MOS capacitor provides a foundation for the basic principles of MOS theory, the semiconductor surface and the oxide aren't perfect. Various charges exist at the interface and in the oxide and a difference in the Fermi levels exist between the metal and the semiconductor. The charge can be categorized into interface trapped charge and oxide charge. Oxide charge include:

- Fixed charge
- Oxide trapped charge:
    - Border traps
    - Bulk traps
- Mobile charge

Trapped charge can cause a shift in the threshold voltage of the transistor. Further, the trapped charge can also change with time which can cause a shift in the threshold voltage over time and result in instability of operating characteristics of transistors. Fixed and trapped charge can both scatter the carriers in the channel, which as discussed previously can lower the carrier mobility. All of the aforementioned non-idealities can result in device failure and breakdown of the oxide [4].

Figure 3.5.1 is an illustration of non-idealities that exist in a MOS capacitor. These imperfections and the effect of the difference in work functions on C-V responses will be described in the next section.

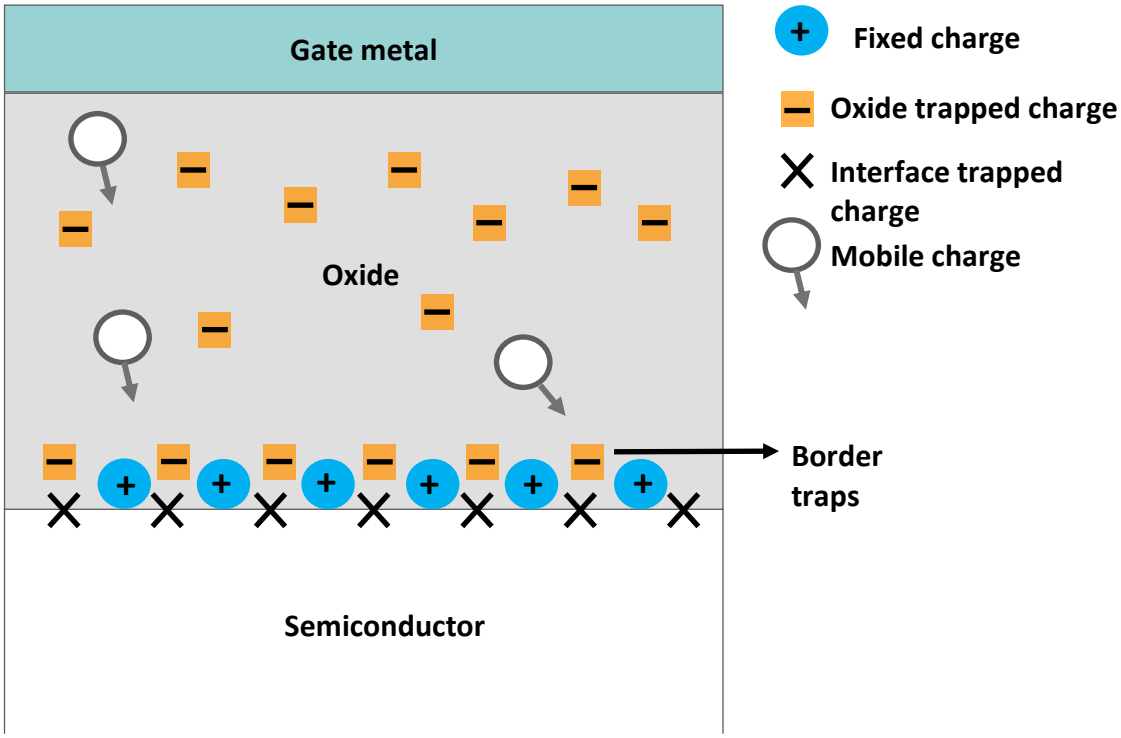



**Figure 3.5.1: A cross-section of an MOS capacitor with defects present**

### 3.5.1 Work function difference

Previously, the work function difference between the metal and semiconductor of a MOS capacitor was defined to be zero, i.e. the Fermi energy (or Fermi level energy) of the semiconductor was equal to that of the metal. ($E_{Fm} = F_{Fs}$). However, this isn't always true, and it depends on the choice of the materials used in the MOS system. If, $\phi_{ms} \neq 0$eV, then on contact electrons flow from the material with high Fermi level energy to the one with the lower until the Fermi levels are equal. Now, when the applied bias is zero the bands are already bent resulting in the band diagram shown in Figure 3.5.2. It can be observed that the flat band voltage now has been shifted by an amount equal to $\phi_{ms}$ , ergo, in the absence any defects present, the flat band voltage when $\phi_{ms} \neq 0$eV is given by equation 3.22.

$$V_{fb} = \phi_m - \phi_s = \phi_{ms} \qquad 3.22$$

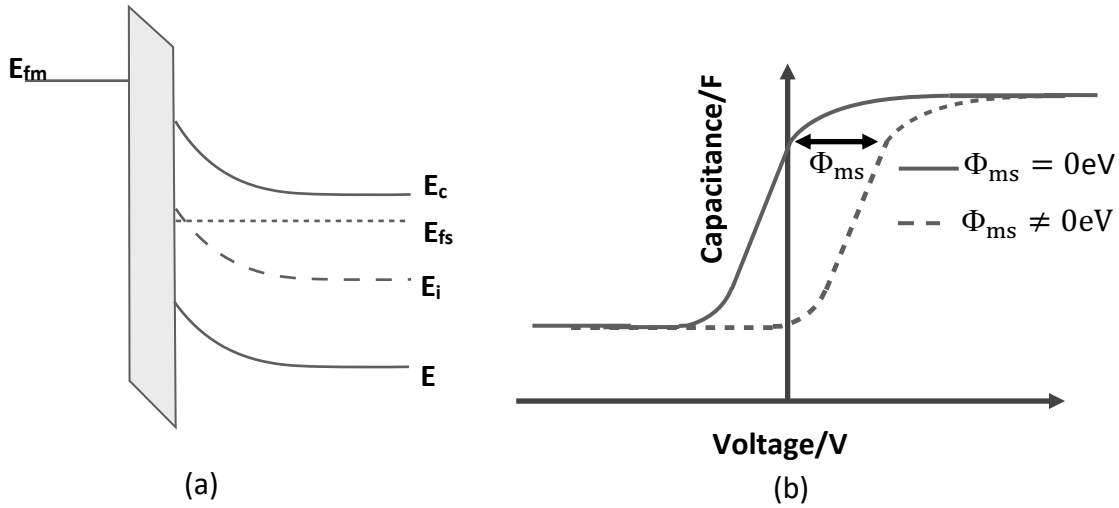



**Figure 3.5.2: (a)Band diagram and (b) Effect of C-V under zero bias when $\phi_{ms} \neq 0eV$,**

### 3.5.2 Interface trapped charge

Interface trapped charges, $Q_{it}$, is located at the oxide-semiconductor interface and originate due to the abrupt termination of the periodic lattice at the surface of a semiconductor [1, 2]. The abrupt termination results in unpassivated bonds known as dangling bonds, which introduce electronic energies at various levels in the forbidden gap as shown on Figure 3.5.3. These states can either be donor or acceptor like in nature. They are donor like if they are positively charged when empty and neutral when full. Acceptor-like states on the other hand are neutral when empty and negatively charged when full.

Interface traps are in electrical communication with the underlying semiconductor and hence vary as a function of band bending. Figure 3.5.4(a) to (c) depicts the effect of interface traps on C-V curves. These include a stretch in the C-V curve, a hysteresis between the forward and backward sweep and also a dispersion in the curves when measuring C-V at different applied frequencies.

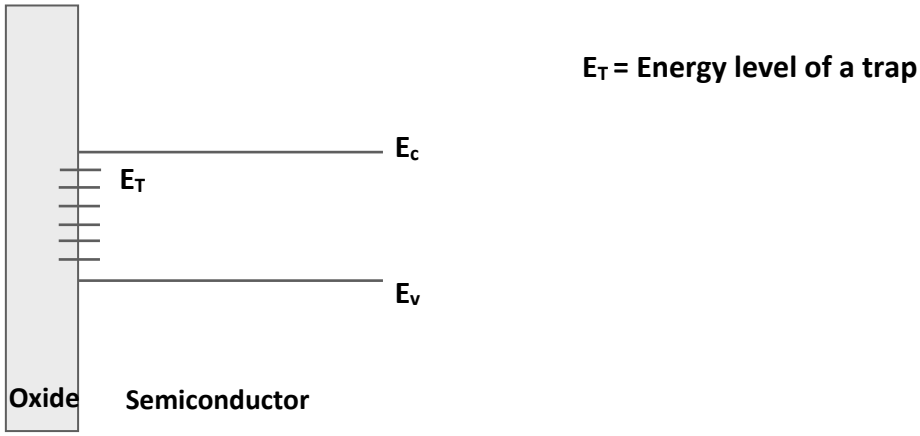



**Figure 3.5.3: Band diagram containing traps with different electronic energies present in the forbidden gap**

### 3.5.2(a) Stretch in C-V

Charge neutrality requires that a change in the gate charge, $\delta Q_G$ is balanced by an amount $\delta Q_s$ in the semiconductor, which is achieved by a change in the band bending. However, in a system with interface traps, a change in the band bending also causes a change in $Q_{it}$. Therefore, the required change $\delta Qs$ is less. Hence, a larger range of bias voltage is required, causing the C-V curve to stretch out along the bias axis as illustrated in Figure 3.5.4(a) [2].

$$\delta Q_G + \delta Q_S = 0 \text{ C/cm}^2 \quad 3.24$$

$$\delta Q_G + \delta Q_S + \delta Q_{it} = 0 \text{ C/cm}^2 \text{ [2]} \quad 3.25$$

### 3.5.2(b) C-V hysteresis and frequency dispersion

Equation 3.26 gives the characteristic time, $\tau$ with which a free charge in a semiconductor gets trapped by a trapping state of energy $E_T$. Interface traps can give rise to C-V hysteresis between the forward sweep, when the voltage is swept from negative to positive and backward sweep, when the voltage is swept back to the initial negative voltage, due to the trapping and de-trapping mechanisms of carriers when swept from one direction to the other [5].

As can be noticed $\tau$ is a function of the distance of the trap from the majority carrier band edge. As the frequency of the signal is decreased, the period of the signal is increased. This allows carriers to get trapped with energy levels located at distances further from the carrier band edge. And results in a frequency dependent dispersion in the C-V curves.

$$\tau = \frac{1}{\sigma V_{th} N} \exp\left(\frac{\Delta E}{k_B T}\right)^{[6]} \quad 3.26$$

$\Delta E = E - E_T$
$E =$ Enery of the majority carrier band edge, $E_T =$ trapping state energy
$\sigma =$ capture cross section, $v_{th} =$ thermal velocity,
$N =$ density of states in the majority carrier band, $k_B =$ Boltzmann constatnt,
$T =$ temperature

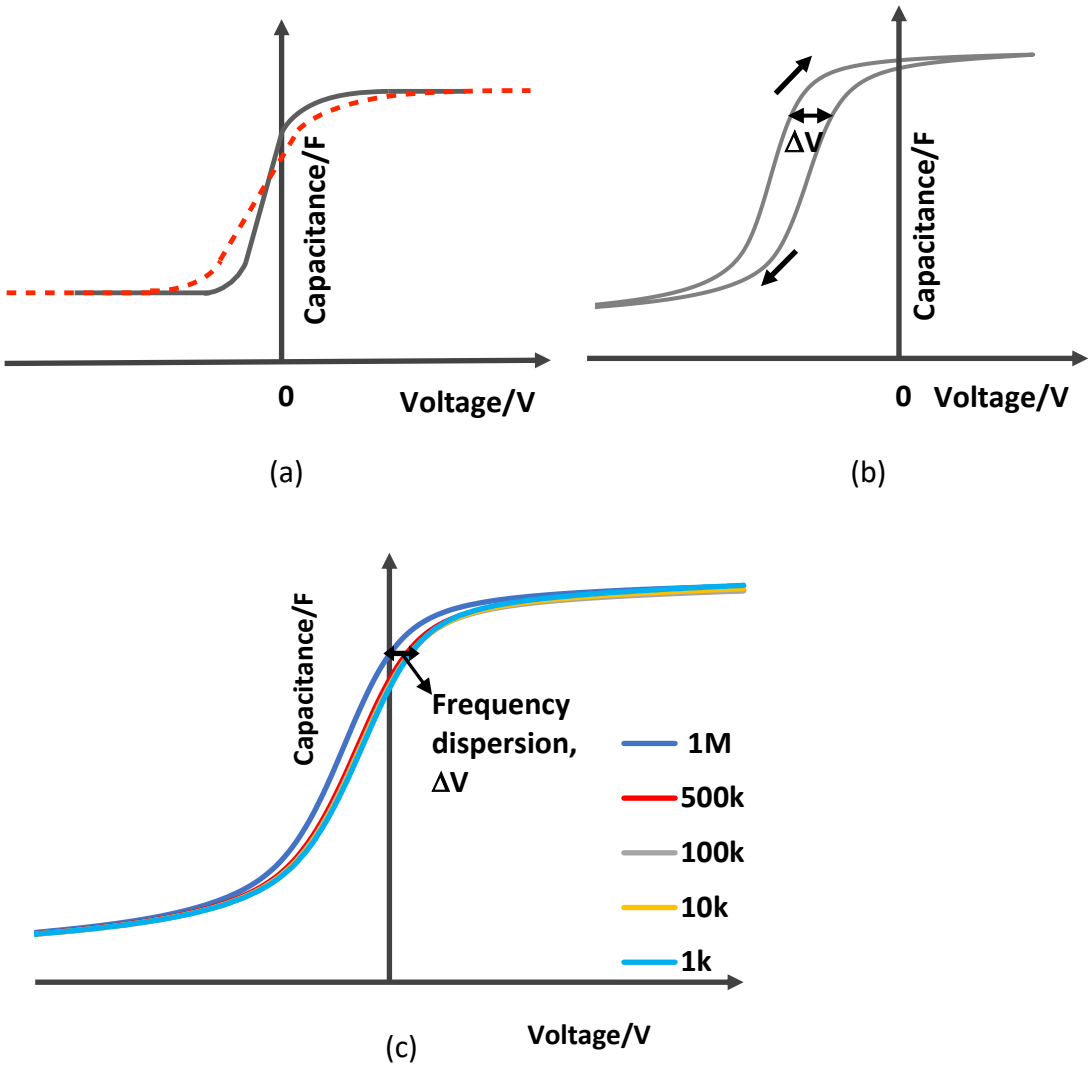



**Figure 3.5.4: (a) C-V stretch out, (b) C-V hysteresis and (c) Frequency dispersion in MOS capacitors with interface traps**

### 3.5.3 Fixed charge

Fixed charge is located at the semiconductor-oxide interface and is invariant to the bias voltage. However, the presence of fixed charge can cause a shift in the CV curve as demonstrated in Figure 3.5.5. The direction of translation depends on the polarity of the

charge, where negative charge results in a positive shift and vice versa [7]. In the presence of only fixed charge, equation 3.27, shows the effect of the change in flat band voltage from that of an ideal MOS capacitor.

$$\Delta V_{fb} = -\frac{Q_f}{C_{ox}} \qquad 3.27$$

$Q_f$ = Fixed charge density

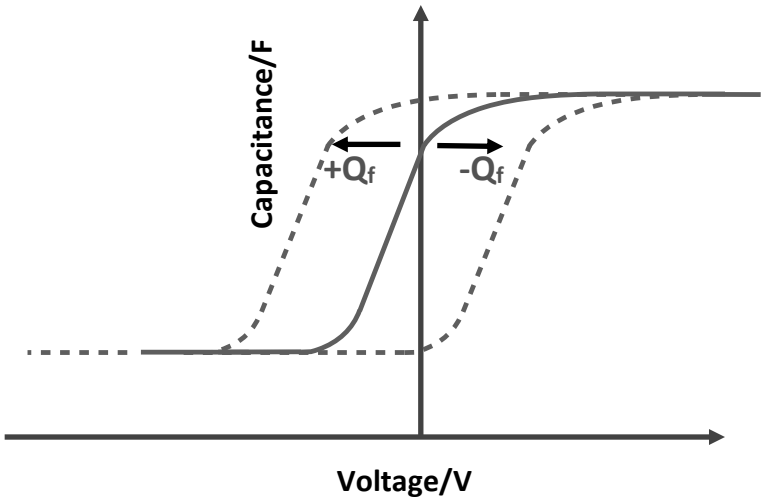



**Figure 3.5.5: Effect on C-V due to fixed charge**

### 3.5.4 Oxide trapped charge

Oxide traps are divided in to two types; border and bulk traps [8][9]. Border traps lie very close to the semiconductor-oxide interface while bulk traps exist further into the oxide. [10].

### 3.5.4(a) Border traps

Border traps are near-interfacial oxide traps and can exchange charge with mobile carriers in the semiconductor bands through tunnelling [10]. Like interface traps, they too are in electrical communication with the underlying semiconductor, however their trap time constants increase as a function of distance from the oxide-semiconductor interface, resulting in the number of traps participating to decrease exponentially. This gives rise to the equation 3.28. An example of border traps in accumulation is shown in Figure 3.5.6. In the depletion region, because the tunnelling time would be extremely large due to low electron density, the border traps have minimal impact [11].

$\tau(x) = \tau_0 e^{2\kappa x}$ [12]

$\tau_0$ = trap time constant = $\frac{1}{\sigma v_{th} N_s}$ 3.28

$\kappa =$ attenuation coefficient , $x =$ trap distance from the interface,

$N_s =$ Density of carriers at the surface

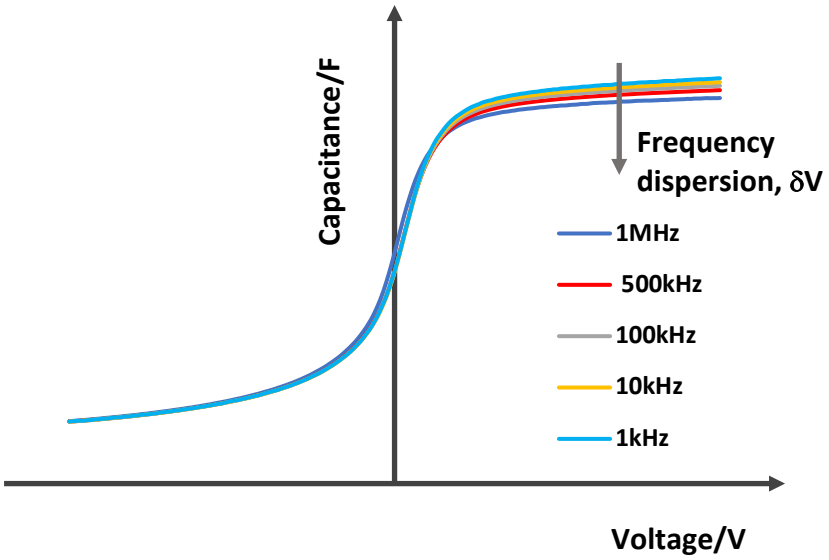



**Figure 3.5.6: Frequency dispersion at accumulation due to the presence of border traps**

### 3.5.4(b) Bulk oxide traps

Bulk oxide traps reside far from the semiconductor surface and therefore do not communicate with the underlying semiconductor [8]. Their effect on C-V is similar to that of fixed charge, resulting in the shift of the C-V curve, represented by equation 3.29.

$$\Delta V_{fb} = -\frac{Q_{ot}}{C_{ox}} \qquad 3.29$$

$Q_{ot} =$ oxide trapped charge

### 3.5.5 Mobile charge

Mobile charge results due to ionic impurities [1][2]. It is referred to as mobile because these charges drift under bias and translate the curve by changing the flat band voltage by an amount shown in equation 3.30.

$$\Delta V_{fb} = -\frac{Q_m}{C_{ox}} \qquad 3.30$$

$Q_m =$ mobile charge

Therefore, the total change in flat band voltage in the presence of non-idealities is the sum of the work function difference and the total shifts due to fixed, bulk oxide and mobile charge, shown in equation 3.31.

$$\text{Total } \Delta V_{fb} = \phi_{ms} - \left(\frac{Q_f}{C_{ox}} + \frac{Q_m}{C_{ox}} + \frac{Q_{ot}}{C_{ox}}\right) \qquad 3.31$$

## 3.6. Summary

The chapter has explained the electrostatics of ideal MOS capacitors and its effect on C-V curves at different biasing regimes. However, as described previously the oxide and the oxide-semiconductor interface are never perfect, and this results in the presence of various charges. These charges have been categorized and their consequence on C-V have also been described.

## 3.7. References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# 4. Fabrication techniques

## 4.1 Introduction

Fabrication techniques are essential when creating devices and the procedures undertaken when producing devices differs depending on the material used and the type of device to be made. This chapter provides an overview of the techniques that were used as part of the MOS capacitor fabrication in this work**.** These techniques include optical lithography, semiconductor material growth, dielectric and metal deposition, semiconductor and dielectric etching and annealing. Information is also provided on the apparatus used to carry out these fabrication techniques, and comparisons to other processes are given as background. A summarised process flow of the processes used to fabricate MOS capacitors in this work is shown in Figure 4.1.1 and the detailed process flow is given in Appendix A.

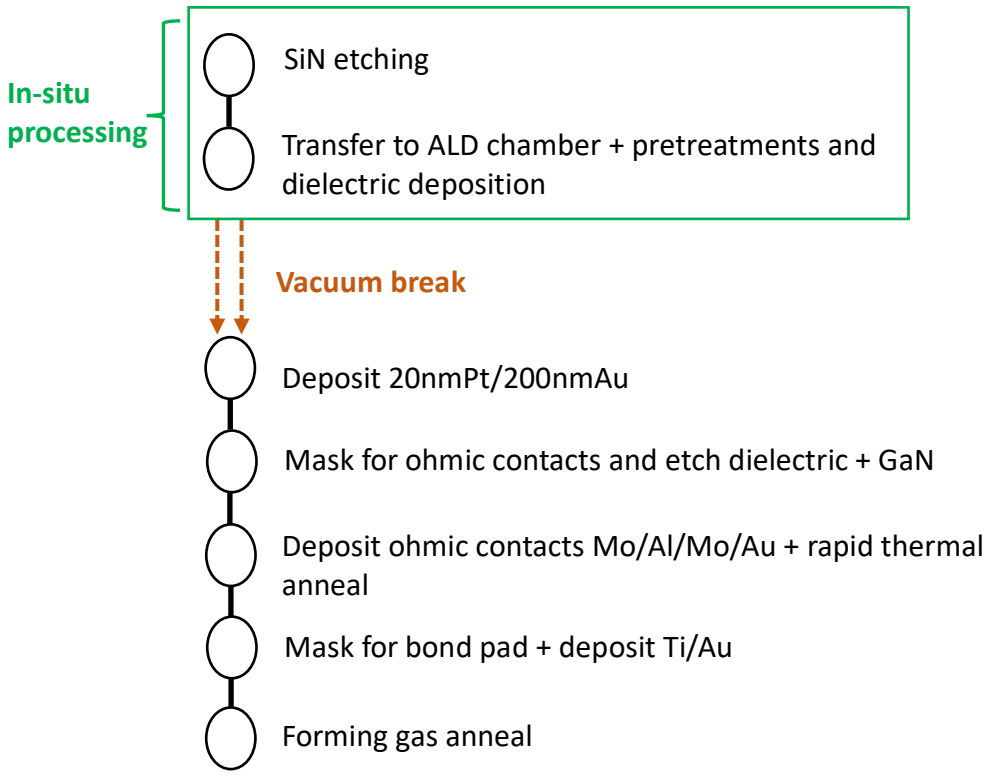



**Figure 4.1.1 Process flow**

## 4.2 In-situ processing

This work has focussed on assessing the electrical performance of MOS capacitors fabricated on a GaN surface that is never exposed to the atmosphere. Therefore, a cluster tool which has the ability to perform in-situ plasma etching and ALD has been utilized. To

facilitate in-situ processing, the MOCVD grown MOS capacitor wafers used in this study included a 5nm silicon nitride ($SiN_x$) cap grown on GaN as the final material deposited in the wafer growth. The SiN was first etched in the plasma etch chamber of the cluster tool before being transferred under vacuum to the ALD chamber where various plasma pre-treatments and dielectric and gate metal were deposited. An Oxford Instruments Plasma Technology Ltd FlexAl ALD system and a Cobra (RIE-ICP) etch system were used in the cluster tool which is illustrated in Figure 4.2.1. The cluster tool also contained a chemical vapour deposition chamber and a scanning auger system. However, in this work the focus was only on in-situ etching and ALD.

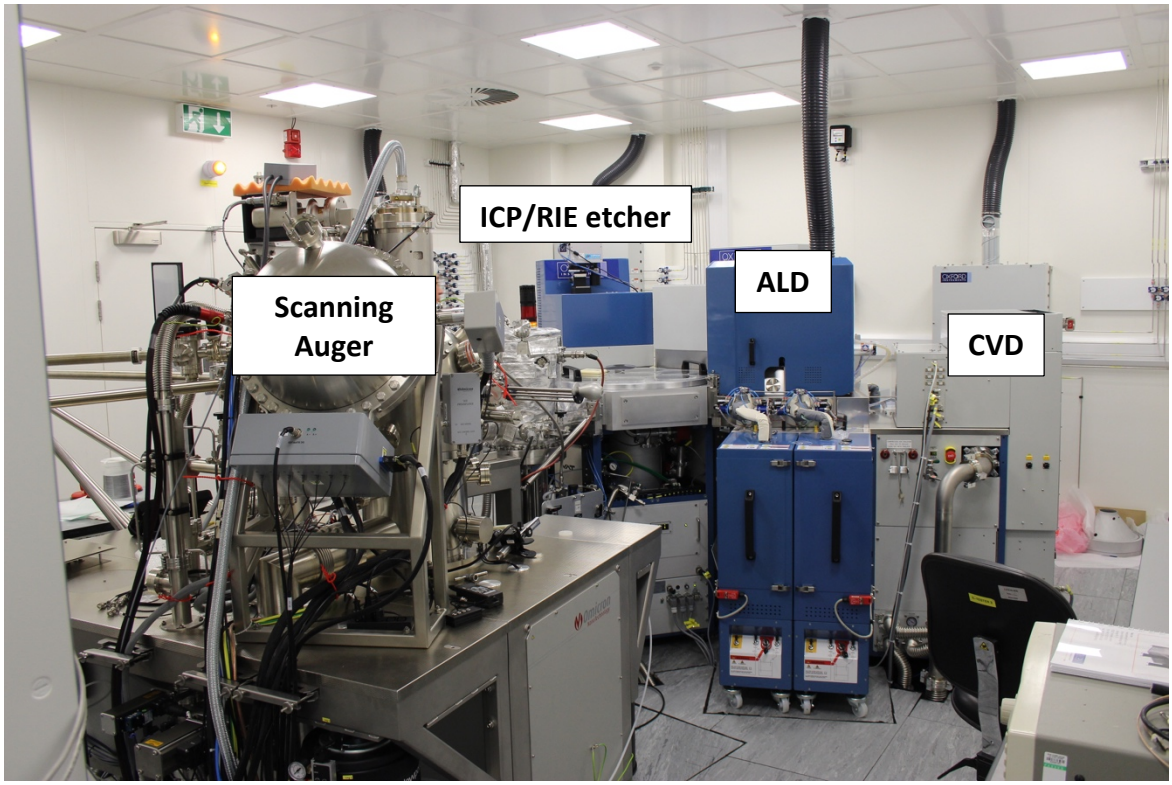



**Figure 4.2.1 Cluster tool**

## 4.3 Film Deposition

For the creation of a MOS capacitor, the techniques of epitaxial growth, dielectric and metal deposition were employed. Although the wafer growth wasn't carried out as part of this research, details of this are given as background in section 4.3(a). The epitaxial growth was carried out using metal organic chemical vapour deposition (MOCVD). Dielectric deposition on the other hand was carried out using atomic layer deposition

(ALD). Metal films were grown using both ALD and electron beam physical vapour deposition (EBPVD). The following sub-chapter describes in detail these different deposition techniques employed for the relevant film growths.

**a. Metal organic chemical vapour phase deposition (MOCVD)**

The deposition conditions and techniques can affect both the structural and electronic properties of material used [1]. The most commonly used techniques for epitaxial growth are molecular beam epitaxy (MBE), MOCVD and hydride vapour phase epitaxy (HVPE). MOCVD has proven to be the preferred technique for gallium nitride growth and has been used to produce the wafers used for this research [1]. MOCVD is a specific type of chemical vapour deposition (CVD) that uses metalorganic precursors in their gaseous form containing the elements of the desired film. Ammonia and trimethylgallium (TMGa) have been used as precursors when growing the GaN wafers used in this work. As described in chapter 2, during CVD growth, films are grown by chemical reactions between precursors that are supplied simultaneously in to a chamber. The basic MOCVD system consist of the following [2] [3]

- Load lock: maintained at high vacuum with a turbo molecular pump, and is used to transfer wafers in/out of the reaction chamber
- Gas handling unit: this system includes the precursors and all of the valves and instruments necessary to control the flow of gases to the reaction chamber
- A reaction chamber: the reactions required for creating the wafers take place in this chamber
- Heating and temperature system: this controls the temperatures in the reaction chamber required for MOCVD reactions
- Exhaust, pumping and pressure controlling system: this includes a vacuum pump for low pressure operation and an exhaust to remove waste products

A schematic of an MOCVD reaction chamber is depicted in Figure 4.3.1.

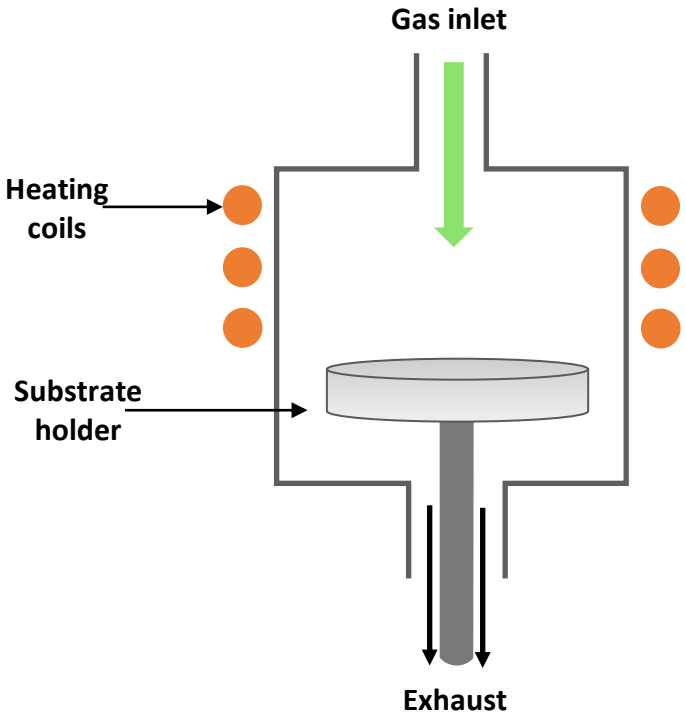



**Figure 4.3.1 Schematic of a metal organic chemical vapour deposition (MOCVD) reaction chamber**

**b. Atomic layer deposition (ALD)**

In this work dielectric and some metal deposition have been carried out using ALD. ALD is a self-limiting sequential growth process where the reactants are exposed to the substrate in separate stages. Additional details of ALD growth, reactors and plasma configurations are discussed in chapter 2.

In this work, an Oxford Instruments Plasma Technology FlexAL system has been used to perform ALD. The ALD chamber has also been used to perform plasma pre-treatments on the GaN surface prior to dielectric deposition. The dielectrics grown were aluminium nitride (AlN) and aluminium oxide ($Al_2O_3$). Titanium nitride (TiN) was also grown by ALD as a gate metal contact and compared with gate metals deposited using E-beam evaporation.

**c. Electron-beam physical vapour deposition (EBPVD)**

Electron-beam physical vapour deposition (EBPVD) also referred to as E-beam evaporation has been used to deposit the gate metal, ohmic metal and low resistance bond pad metallisation.

E-beam evaporation is a form of physical vapour deposition technique where the required material is transported to the substrate in its vapourised form in a vacuum chamber.

A beam of electrons is accelerated from a cathode using high accelerating voltage between 3-40kV towards a crucible containing the material to be deposited [4]. Upon striking the source material some of the kinetic energy of the electrons is converted to thermal energy that heat up the material causing it to evaporate or sublimate [4]. The vapourised material then coats the substrate. The crucible used in the evaporation tool in this work is water cooled to ensure that the electron beam doesn't melt the crucible and give rise to contaminations. A schematic of an E-beam evaporation tool is shown in Figure 4.3.2. Initially the source shutter is opened and the crystal monitor measures the deposition rate. The substrate shutter is opened when the desired evaporation rate is reached allowing the material to be deposited on the substrate.

The metals used for the gate contact are 20nm platinum and 200nm gold. Platinum was chosen because it has a high work function of 5.65 eV. To ensure normally off operation of transistors, threshold voltages above zero are desirable. The work function of the gate metal affects the threshold voltage of the completed transistors and a high work function ensures higher threshold voltages. Gold was used to make contact to the gate metal as it does not oxidise [4]. The ohmic contacts used in this work follow a process which was developed by Dr Xu Li. The ohmic constacts consist of a stack of 10 nm molybdenum/ 40nm Aluminium/ 20nm molybdenum/ 30nm gold. This stack was used because it could be annealed at a lower temperature compared to existing ohmic contacts such as Ti/Al/Ni/Au which are annealed at 770$^{\circ}$C. Therefore, it protects the oxide from thermal degradation. The low resistance bond pad consists of 20nm titanium and 200nm gold. A Plassys MEB 450 and Plassys MEB 550 have been used as evaporation tools in this work.

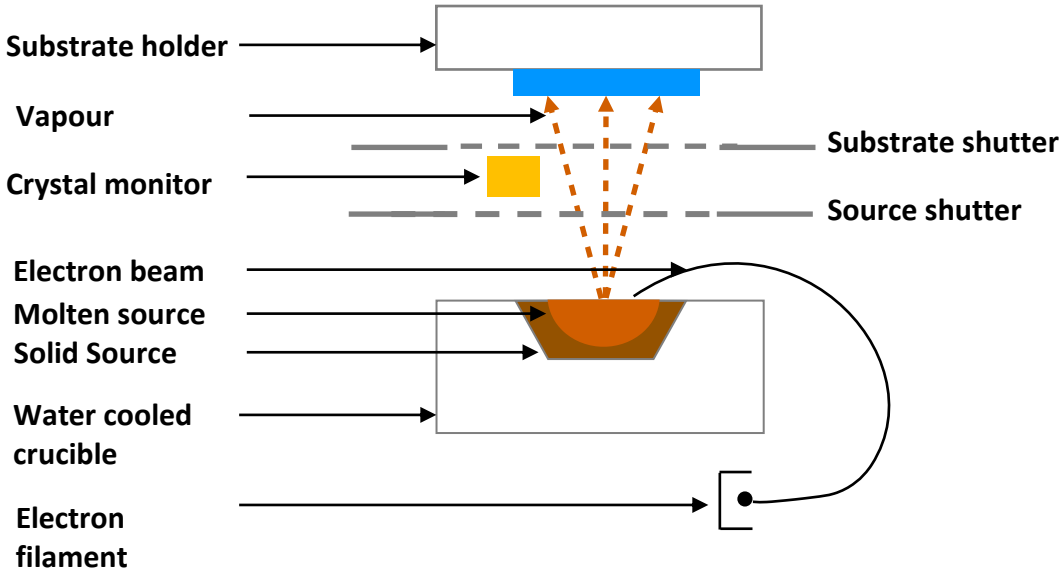



**Figure 4.3.2: Electron beam physical vapour deposition schematic**

## 4.4 Optical lithography

Lithography is the process of defining patterns to enable subsequent selective removal or deposition of materials from or to a substrate. This work uses optical lithography to pattern the areas where the ohmic contacts and vias (which are used to make contact through subsequently deposited dielectric passivation layers), will be deposited.

**The following definitions describe the terminology used in fabrication processes:**

- Photoresist: An organic polymer which changes its chemical structure upon exposure to ultraviolet light (UV) [5]
- Photomask: Consists of a fused silica (QZ) or, glass (SL) substrate coated with an opaque film into which the required patterns are etched producing areas that will let light though [6].

Optical lithography, also known as photolithography defines patterns on a substrate coated with photoresist by using ultraviolet (UV) light. The patterns are generated using a photomask placed on top of the substrate**.** Photoresist is available in two type; positive resist which when exposed weakens the chemical structure of the polymer bonds and becomes easily soluble with developer and negative resist which when exposed polymerises and is insoluble in developer [7]. Figure 4.4.1 illustrates the outcome of using

the two different types of resist However, in this work only positive photoresist has been used, namely S1818 and LOR. A bilayer of S1818 and LOR are used in a process known as lift-off used when depositing ohmic contacts. In this process LOR is developed separately from S1818, the LOR undercuts the S1818 which allows the solution used to remove resist to remove the LOR, S1818 and metal deposited on top more easily. This process ensures that the metallisation is removed where it is not desired.

Listed in order below are the steps undertaken during the photolithography process [8]:

1. Resist coating: resist is applied to the substrate by spin-coating, this involves pouring the resist solution on to the substrate and rapidly spinning it until it is evenly coated. The spinning is performed using an electronic vacuum chuck which spin at 3000-7000 rpm.
2. Baking: this is done after the resist is spun on to the sample in an oven or on a hot plate to improve adhesion and to evaporate solvents in the resist.
3. Exposure: this involves irradiating the resist on the sample through a photomask with UV light
4. Developing: the exposed substrate is placed in a solvent that selectively dissolves areas that have been exposed (positive photoresist)/ unexposed (negative photoresist) to UV light.

Three kinds of photolithography exposure techniques exist; contact, proximity and projection lithography. During contact lithography the mask is in direct contact with the underlying sample while in proximity lithography the mask is approximately 20-30µm away from the substrate. In projection lithography the mask is far away from the substrate and a projection lens system between the wafer and the photomask generates the pattern on the substrate [9]. In this work, contact lithography, represented schematically in Figure 4.4.2, using a Suss Micro tech MA6 tool, has been used to define MOS capacitors.

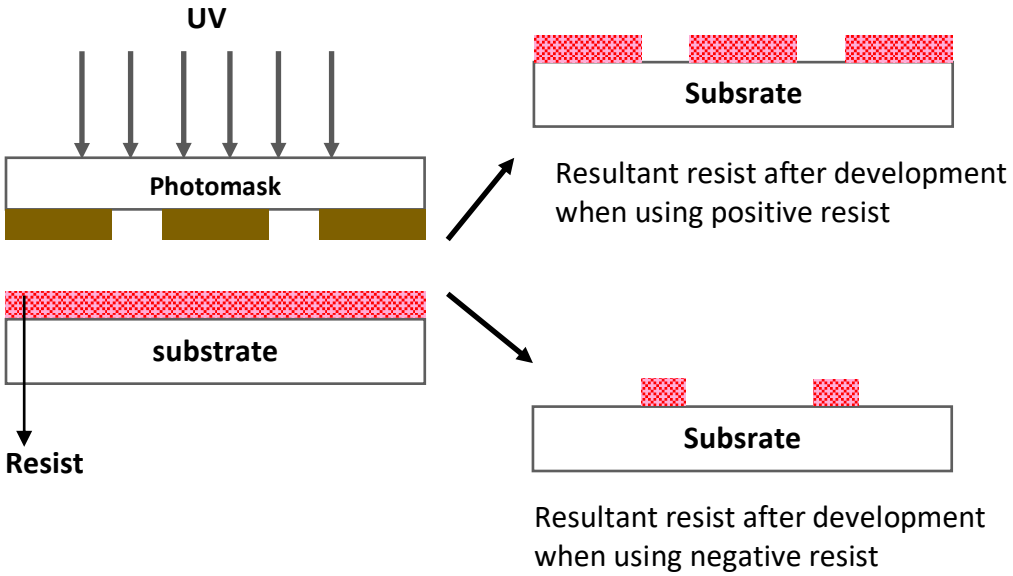



**Figure 4.4.1: Photoresist exposure**

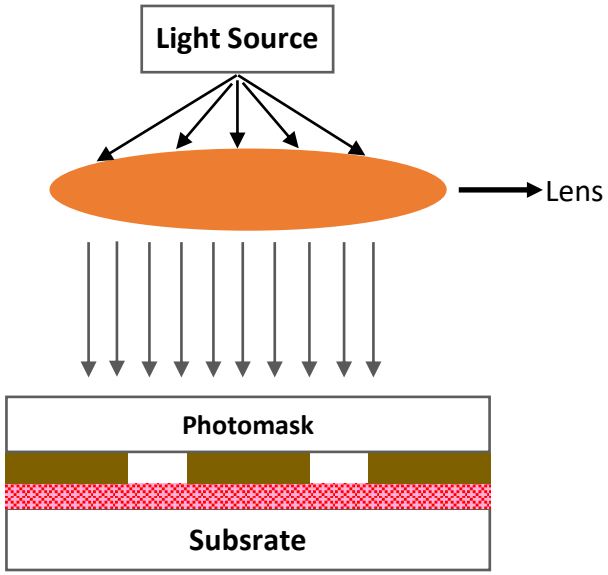



**Figure 4.4.2: Contact photolithography**

## 4.5 Film Removal

Film removal, also referred to as etching, is the process of removing material from a sample. Etching can be split into two distinct areas: Wet etching, and dry etching. In wet etching, etchants used to remove material from the sample surface are liquid solvents. Dry etching as the name suggests, is the process of film removal in the absence of any liquid solvents. These approaches will be described in detailed below. Although in this work only dry etching techniques have been used, the background on wet etching is also given as a comparison.

The parameters investigated when validating an etch include: [9]

- Etch rate: used to determine the time taken to perform an etch of a given depth
- Selectivity: the ratio of the depth of the material etched relative to that of the photoresist mask
- Damage: crystal defects on the surface of the substrate result from high ionic impacts from dry etching [10]
- Etch profile: defines the angle between the horizontal base of the etch and the upright wall and therefore gives an indication of the directionality of the etch [10]. An isotropic etch etches in all directions, while an anisotropic etch, etches in one direction.

**a. Wet etching**

In wet etching the sample is immersed in a liquid in order to carry out etching. Wet etching process can be described by a three stage process:

1. Diffusion of reactants on to the substrate
2. Reaction between liquid etchant and the substrate
3. Diffusion of by-products in to the liquid

**b. Dry etching**

In dry etching, reactive species created in a plasma are used to carry out the etch process. The plasma is a partially ionised gas with a mixture of electrons, ions, radicals and neutral species [9]. A dry etching process can be either a physical (i.e. sputtering) or chemical etch. The former consists of molecules being stripped off by the impact of ions on the wafer while the later uses chemical reactions between the etchant(s) and the sample to remove material [10][11].

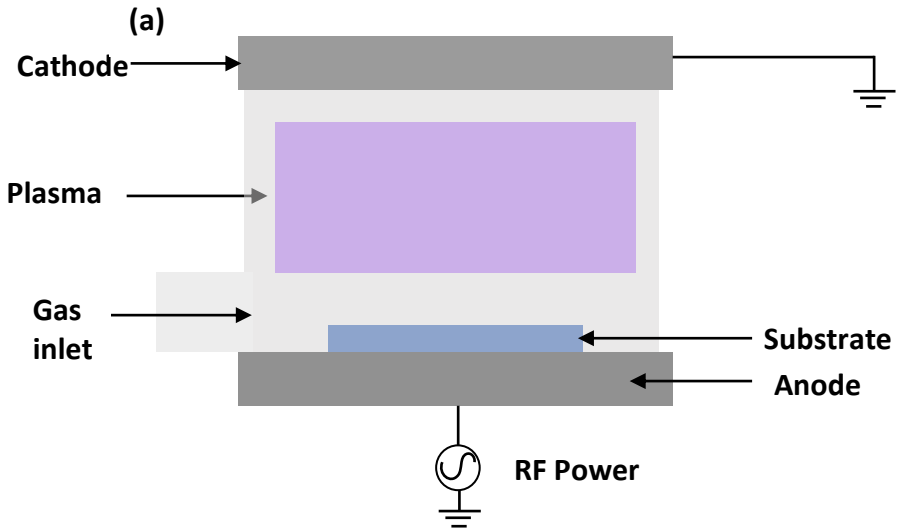
During dry etching the following fundamental steps take place [13]

- The etchant species is generated in the plasma.
- The reactant is diffused through a gas to the etching surface.
- The reactant is adsorbed to the surface if the process is a chemical etch.
- Chemical reactions and/or physical processes occur on the surface to form volatile compounds.

- In chemical etch processes the volatile compounds are desorbed while in physical etch processes the material is sputtered off from the surface and pumped out of the system.

Plasma etch reactors include reactive ion etching (RIE) and inductively couple plasma (ICP) sources or a combination of the two; ICP-RIE. An RIE chamber, depicted in Figure 4.5.1(a) uses a capacitively coupled plasma (CCP) source where the plasma is generated by applying RF power to a cathode while grounding the counter electrode where the substrate is placed [10] [11]. In an ICP chamber on the other hand plasma is generated inductively; i.e., the plasma is created by electric currents which are produced by time varying magnetic fields. As illustrated in Figure 4.5.1(b) this system uses two RF sources, where the power from one is inductively delivered to the plasma while the other is connected to the substrate and capacitively controls the ion energy plasma.

In this work dry etching is used to produce recessed ohmic contacts, where 600nm of GaN is etched aniosotropically using silicon tetrachloride ($SiCl_4$) at applied power of 100W, pressure 8mTorr and 100sccm gas flow. Dry etching is also used post resist development to remove any resist residue using an oxygen plasma with a low power of 10W, a pressure of 50mTorr and a flow of 10sccm.



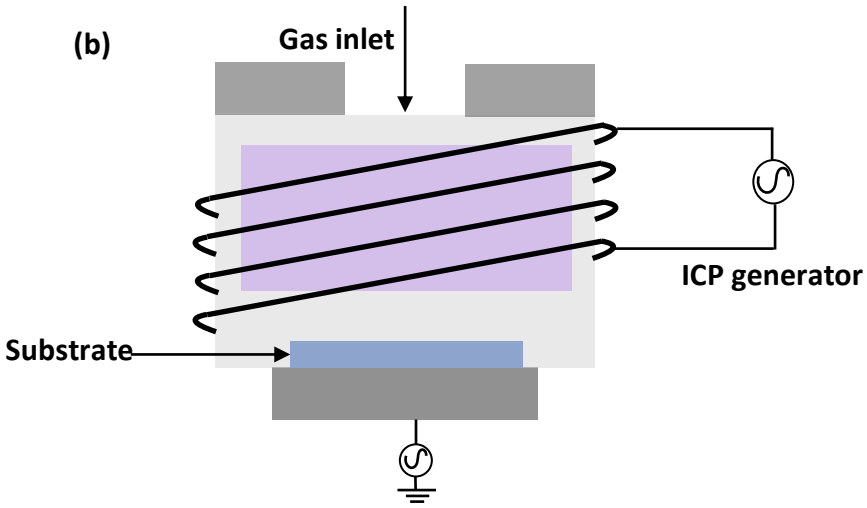



**Figure 4.5.1: (a)Reactive ion etching (RIE) source and (b) Inductively coupled plasma (ICP) source**

## 4.6 Annealing

Rapid thermal annealing (RTA) has been used in this work to anneal the ohmic contacts of the MOS capacitors. In an RTA system, a high intensity lamp is used as the heat source. The temperature is controlled by a pyrometer and measured by a thermocouple [15]. During a rapid thermal annealing process the sample is heated at a high temperature for a short period of time. In this work RTA has been used to anneal the ohmic contacts in the presence of nitrogen for two minutes at $550^0$C. Figure 4.6.1 portrays a schematic of an RTA reactor.

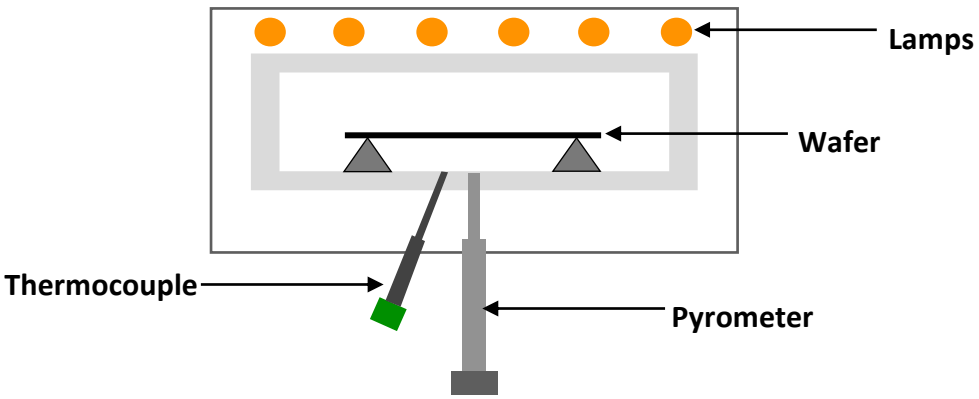



**Figure 4.6.1 Rapid Thermal Anneal (RTA)**

## 4.7 Summary

This chapter has outlined the MOS capacitor fabrication process flow, along with the apparatus used. The fabrication process included optical lithography, film deposition, film removal and annealing. A cluster tool has been utilised to perform in-situ etching and ALD to ensure the GaN surface is never exposed to the atmosphere. The ohmic contacts, vias and gate metal have been deposited using E-beam evaporation and the ohmic contacts have been annealed using a rapid thermal anneal.

## 4.8 References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# 5. Characterisation and metrology

## 5.1 Introduction

This chapter describes the techniques used during this work to analyse the dielectric film quality and the dielectric-semiconductor interface. The thickness and refractive index of the aluminium nitride films deposited are obtained using a spectroscopic ellipsometry. The conduction and valance band offset data between the deposited dielectric film and the semiconductor are determined using x-ray photoelectron spectroscopy. Voltage and frequency dependent measurements of MOS capacitors are used to assess the quality of the dielectric and the dielectric-semiconductor interface. The quality of the metal films grown were tested electrically using both MOS capacitor structures and linear transfer length method (L-TLM) structures. Details of the metrology and measurement techniques are explained in the following sections.

## 5.2 Thin film characterisation and metrology

**Spectroscopic Ellipsometry**

Spectroscopic ellipsometry is used in this work to provide information regarding the thickness and refractive index of the films deposited. Figure 5.2.1 illustrates a schematic of an ellipsometer. It consists of a light source which is passed through a polarizer that allows only linearly polarised light to be incident on the sample. The ellipsometer measures the change in the polarisation of the light which is reflected from the sample of interest [1]. A detector converts the reflected light to electric signals which are compared with the input light signal to produce the amplitude, $\psi$ ratio and the phase shift, $\Delta$.

In order to obtain the thickness and refractive index, the measured data and algorithms are used to generate a mathematical model that describe the interaction of light with the sample [2]. This is then compared to a defined theoretical model. This model consists of the layer structure, thickness and variables that needs to be fitted. These variables are then adjusted until theoretical data fits that of the measured data and the required parameters are then obtained. A Cauchy model was used when measuring the ALD deposited AlN films

described in more detail in chapter 6. This model is used for transparent films and is given by the equation 5.1.

$$n(\lambda) = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^4} \quad 5.1$$

where $\lambda = \text{wavelength}$

A, B and C are the fitting parameters

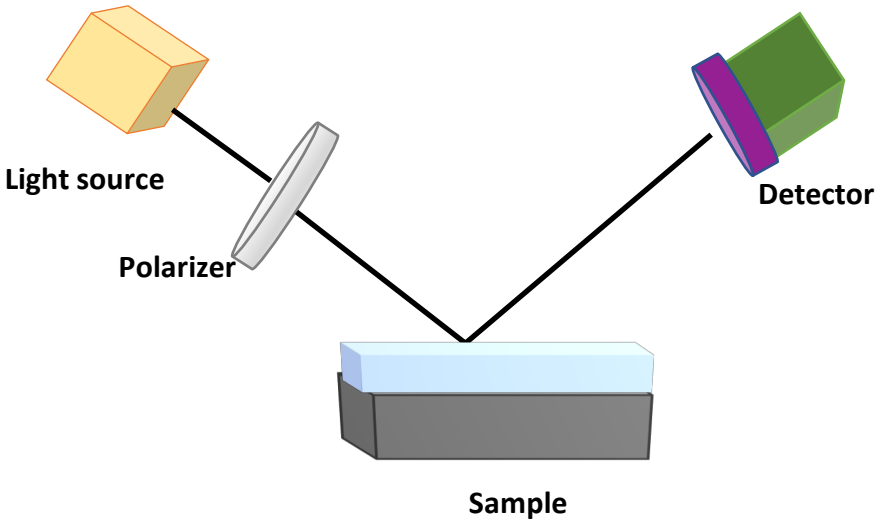


**Figure 5.2.1: Schematic of a spectroscopic ellipsometry**

**X-ray photoelectronic spectroscopy (XPS)**

X-ray Photoelectronic Spectroscopy is a technique that is employed to investigate the chemistry of surfaces [3]. XPS has been used in this work to identify specific elements in AlN films deposited, and also to extract valence band and conduction band offset between AlN and GaN. The XPS measurements in this work have been carried out by collaborators at the University of Liverpool. A schematic of an XPS system is illustrated in Figure 5.2.2. It uses an X-ray source, which is directed towards a sample surface; the energy of the x-ray photon is completely absorbed by the core electron of atoms in the sample. If the photon energy, $h\nu$ is large enough electrons will be able to escape from the atom. The emitted electrons are called photoelectrons and the binding energy of these electrons can be calculated using equation 5.2.

$$h\nu = E_b + E_k + \phi^{[3]} \quad 5.2$$

$$\text{Therefore, } E_b = h\nu - (E_k + \phi)^{[3]} \quad 5.3$$

Where $h\nu = x - ray\ photon\ energy, E_b = binding\ energy,$

$E_k = kinetic\ energy, \phi = work\ function\ induced\ by\ the\ analyzer$

Photoelectrons emitted from the sample of interest are then analysed to study the chemical composition and electronic state of the sample. Each atomic element has a characteristic binding energy that is related to its core atomic level. These energies are displayed as a set of peaks in a photoelectron spectrum. The peaks at particular energies confirm the presence of particular elements.

To obtain the details of band offsets the Kraut method, shown in equation 5.4 was used initially to calculate the valence band offset (VBO) [4]. Literature values were taken for the band gap of the dielectric and the semiconductor. These values will reflect ideal materials and may not represent the actual material qualities in this work, this may lead to small inaccuracies in the calculations. The valence band maximum of these were calculated by linear extrapolation of the leading edge to the baseline of the valence band spectra as indicated in Figure 5.2.3 [5].

$$\Delta E_V = \Delta E_{Cl} + (E_{Cl,GaN} - E_V)^{GaN} - (E_{Cl,Dielectric} - E_V)^{Dielectric} \quad 5.4$$

$\Delta E_v = Valence\ band\ offset,$

$\Delta E_{CL}$

$= Difference\ in\ the\ core\ level\ binding\ energies\ between\ the\ film\ and\ the\ semiconductor$

$E_V = Valence\ band\ maximum$

$E_{Cl,GaN} = Core\ level\ binding\ energy\ of\ GaN$

$E_{Cl,AlN} = Core\ level\ binding\ energy\ of\ AlN$

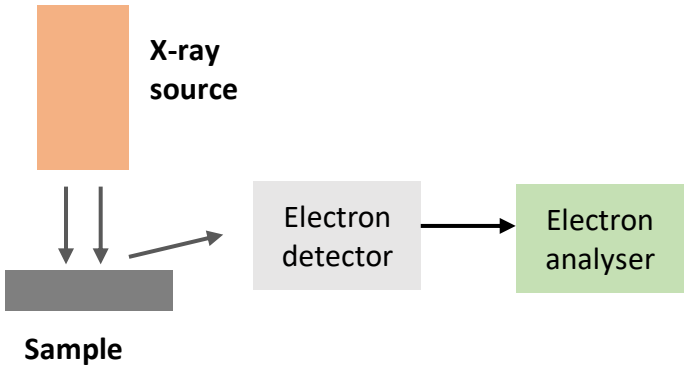


**Figure 5.2.2 Schematic of an XPS measurements set up**

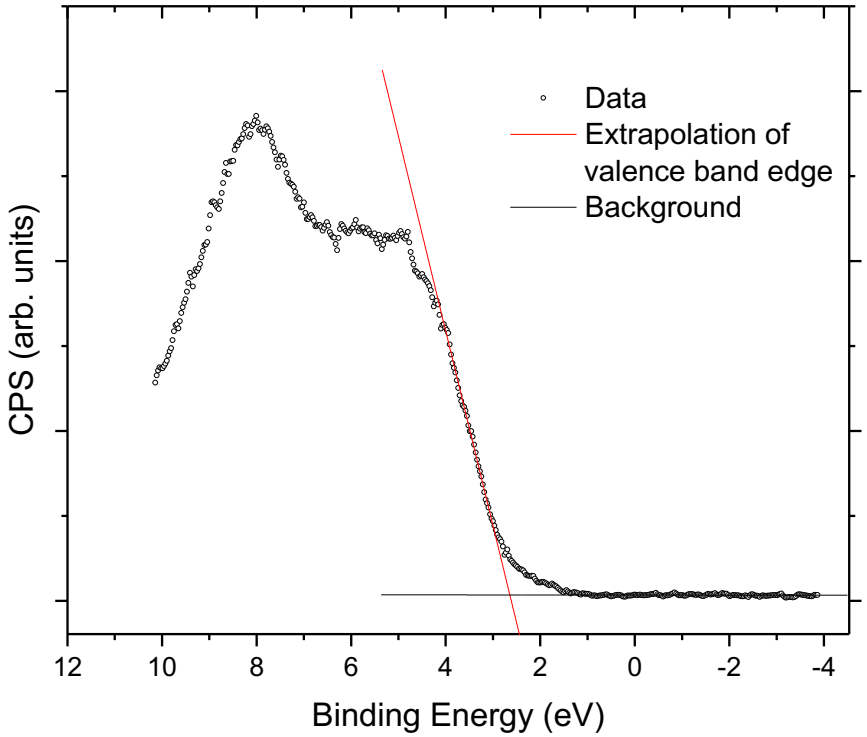


**Figure 5.2.3: Linear extrapolation of valence band edge to determine valence band maximum**

## 5.3 MOS capacitor characterisation

Capacitance-voltage (C-V) measurements give useful information about the internal structure of MOS capacitors. They can be used to identify defects in the dielectric itself and at the dielectric-semiconductor interface. Described below are characterisation methods adopted in analysing the C-V data obtained from the MOS capacitors fabricated in this work.

**Flat band voltage**

The flat band voltage, as described previously in chapter 3 is the voltage at which the surface potential is zero ($\psi_S$ = 0V) and there is no band bending at the dielectric-semiconductor interface. Flat band voltage is an important metric that is used when calculating C-V hysteresis and frequency dispersion which will be discussed in the following subsections. The comparison of an ideal $V_{fb}$ to that of a measured $V_{fb}$ can also give useful information regarding the fixed charge present in dielectric. Winters et al, describes a method where $V_{fb}$ is realised by calculating the point of inflection of C-V curves [6]. In his

work, Winter et al's method has been proven to be equal to the $V_{fb}$ that is obtained when calculating the flat band capacitance, $C_{fb}$. The point of inflection was chosen because mathematically it is the transition point where the shape of the C-V curve changes from convex to concave.

In order to attain the point of inflection the double derivative of the C-V curve is obtained. The point of intersection between C-V and the double derivative gives the point of inflection which is equal to the $V_{fb}$. This is illustrated in Figure 5.3.1.

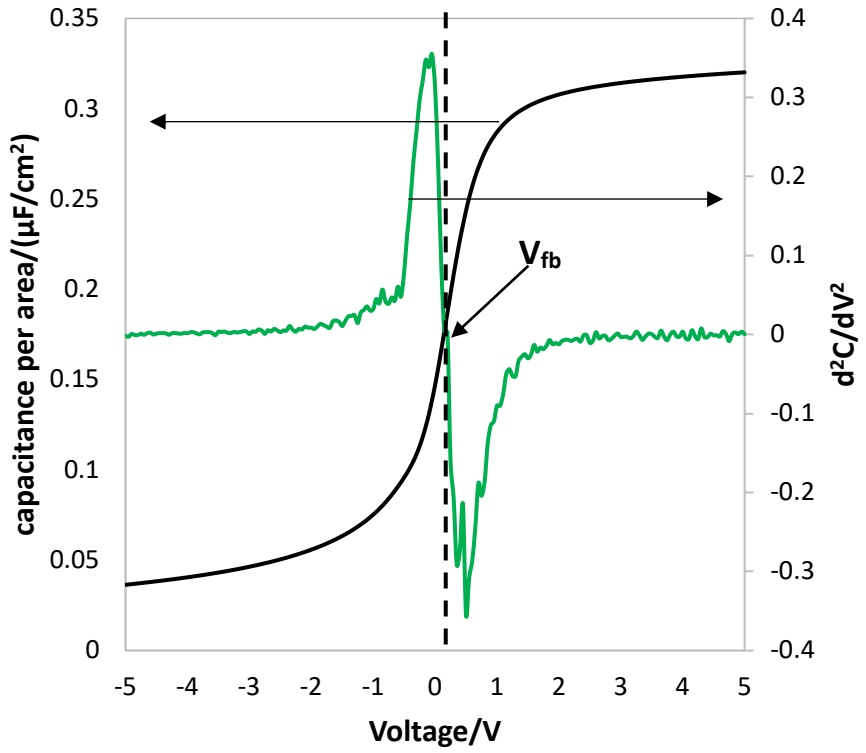


**Figure 5.3.1: C-V curve and double derivative to obtain $V_{fb}$ at point of intersection**

### C-V hysteresis

To obtain the C-V hysteresis,$\Delta_{hysteresis}$ a 1 MHz AC signal, of 20mV amplitude applied on top of a slowly varying DC bias sweep from -5V to +5V and back. The hysteresis is measured by the difference in the flat band voltages in the forward and backward sweep. The flat band voltages are determined by the point of inflection method (as described previously) of the two curves. As explained in chapter 3, hysteresis arises due to the presence of interface traps between the dielectric and the GaN surface. Shown in Figure 5.3.2 is the $\Delta_{hysteresis}$ obtained between the forward and backward C-V sweep.

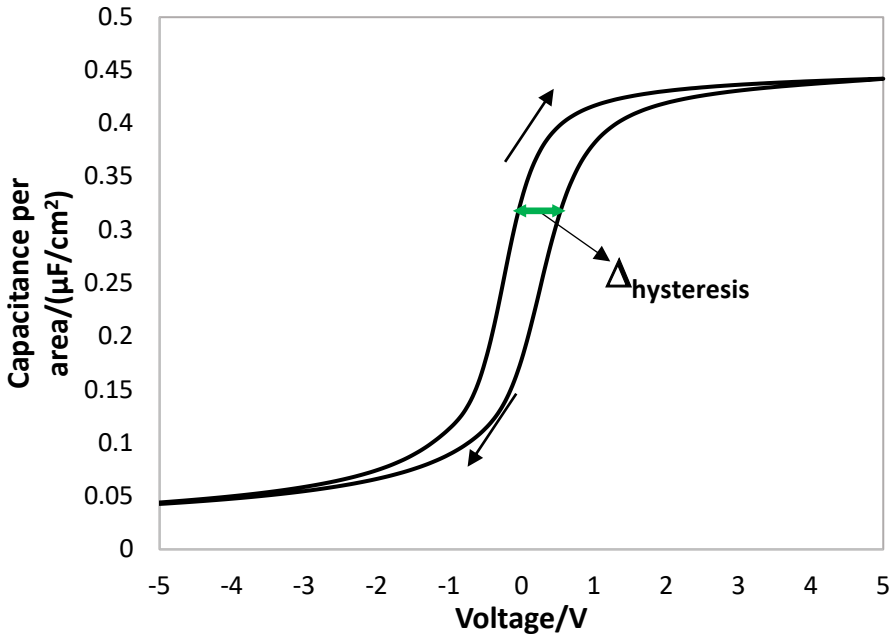


**Figure 5.3.2: C-V hysteresis obtained during forward and backward sweep**

**The frequency dispersion**

To obtain the frequency dispersion, $\Delta_{dispersion}$ the C-V curves at frequencies ranging from 1MHz to 1kHz were measured. Illustrated in Figure 5.3.3 are the C-V curves measured at the various frequencies shown on the legend. The $\Delta_{dispersion}$ reported in the work is the maximum difference in the flat band voltage obtained between the different frequencies. The $V_{fb}$ at different frequencies were again calculated using the method described previously.

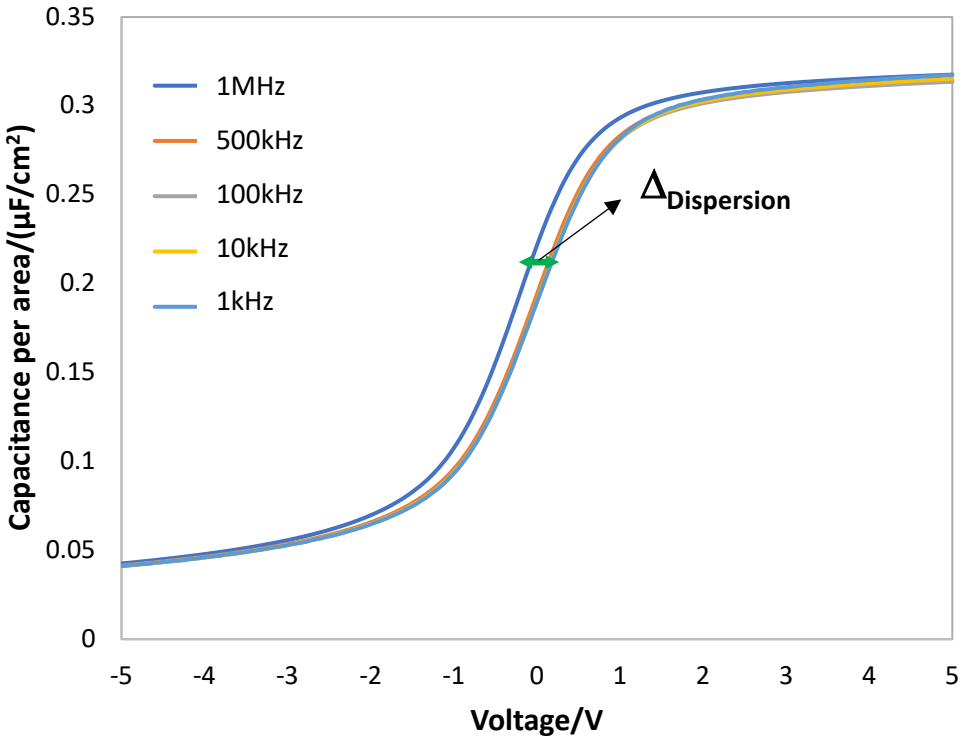


**Figure 5.3.3: Frequency dispersion obtained at frequencies ranging from 1MHz -1kHz**

**Stress voltage measurements**

During the stress voltage measurements, the C-V curve is swept forwards and backwards while increasing the range of sweep by 1V with every measurement. i.e. the curve is swept from -5 V to 0V and back to -5V and then -5V to 1V and back to -5V and so on. The hysteresis at each range is calculated using the difference in the flat band voltage as outlined above. The increase in hysteresis with the increasing voltage range is indicative of an increase in interface trap generation. Figure 5.3.4 illustrates the curves obtained during a measurement of this type.

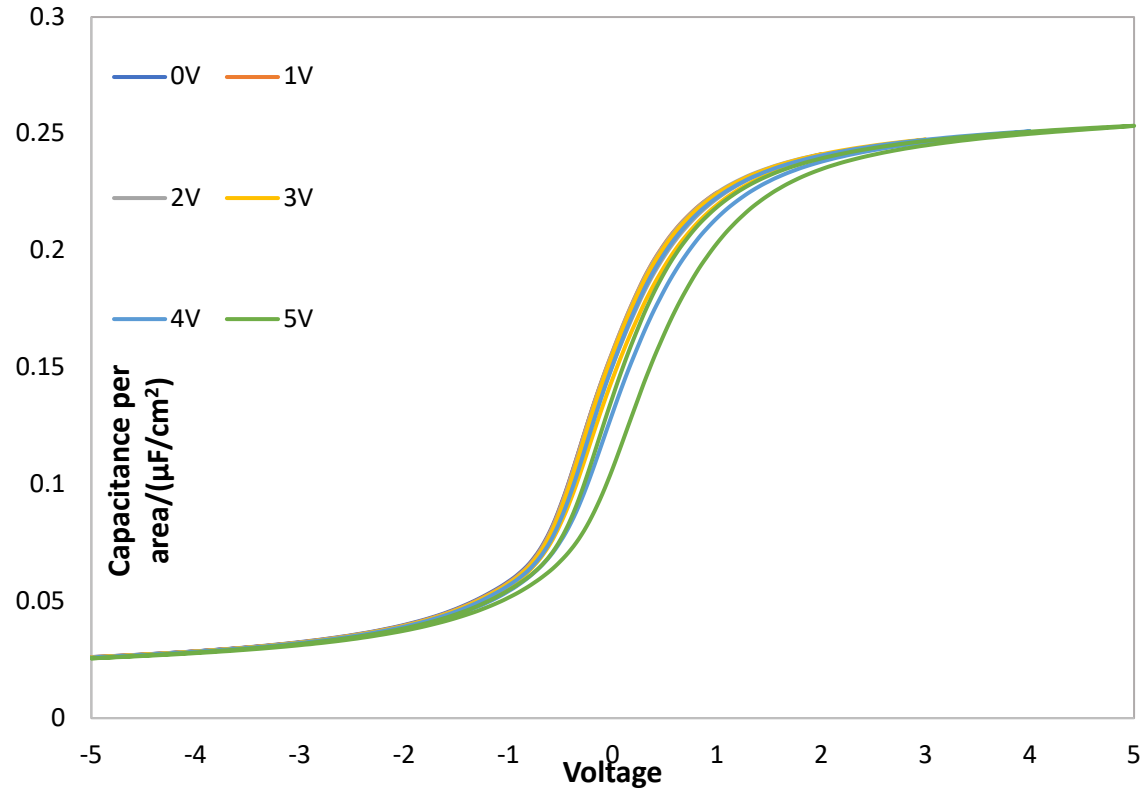


**Figure 5.3.4: C-V hysteresis obtained at different voltage ranges**

**C-V stretch out**

The stretch out of the C-V curve is determined by obtaining the first derivative of the 1 MHz C-V curve. It is measured at 1MHz to ensure that the C-V response is not affected by high number of traps at lower frequencies. The maximum slope indicates the stretch out of the curve; i.e., the higher the slope the lower the stretch out and the lower the number of trapping states that are being accessed. Figure 5.3.5 illustrate the dC/dV curve obtained when the C-V curve is differentiated.

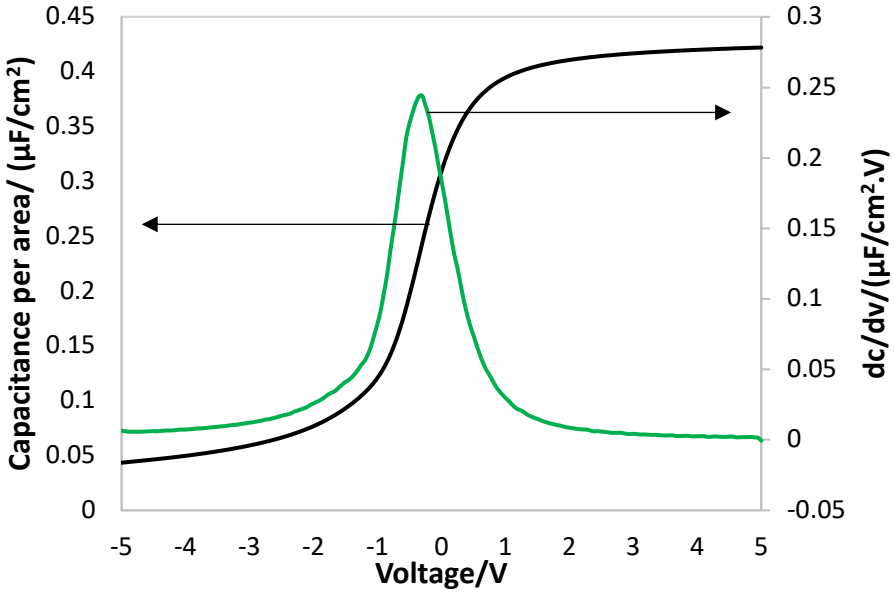


**Figure 5.3.5: C-V curve and slope obtained to provide C-V stretch out**

**Breakdown and leakage**

Breakdown voltage and leakage currents are measured by varying the applied voltage and measuring the current flow. Breakdown is defined as the voltage that occurs when there is a large increase in current flowing in the oxide [7]. When a dielectric is stressed by a voltage it loses its insulating properties due to the generation of traps. Percolation theory suggest that the breakdown occurs from a conduction path that is created from these as a consequence of the increased number of traps [8][9]. This gives rise to catastrophic breakdown of films. Figure 5.3.6 illustrates an I-V curve that is measured to obtain breakdown and leakage properties. The leakage value obtained is the current that flows through the dielectric at 1V.

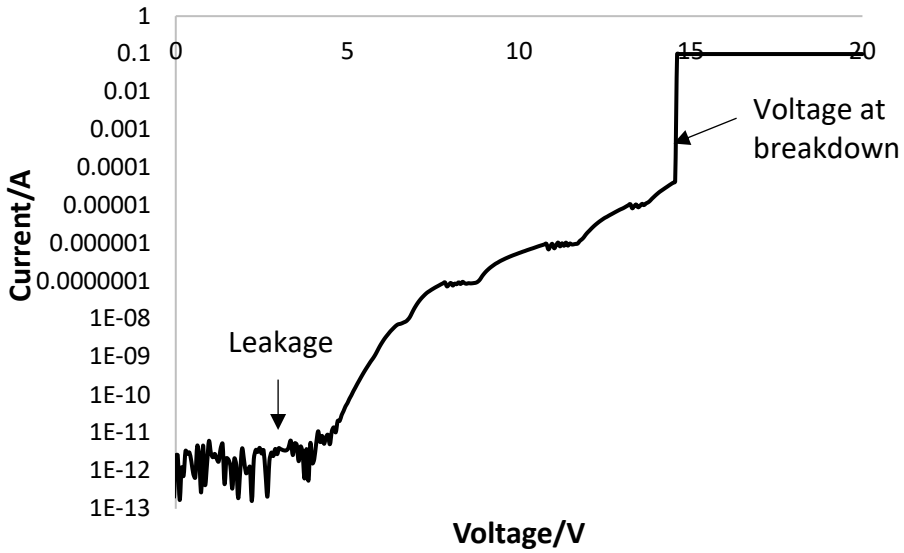


**Figure 5.3.6: Current vs voltage measured to obtain breakdown and leakage currents**

# 5.4 Characterisation of sheet resistance and resistivity

**Sheet Resistance and resistivity**

The sheet resistance of the titanium nitride grown in this work was evaluated using the Transfer Line Method (TLM). These measurements were used to extract the sheet resistance ($R_{sheet}$) and resistivity, ρ of the TiN deposited. Linear TLM structures illustrated in Figure 5.3.7(a) were used and they consist of identical contacts with different spacing, $L_i$ in between. The total resistance, $R_T$ measured between the contacts consists of the top metal contact $R_m$, the resistance of the underlying material $R_x$ and also the contact resistance, $R_c$ between the metal and the underlying material [3]. $R_T$ is therefore the sum of $R_m$, $R_x$ and $R_c$ and is given in equation 5.5. $R_x$, the resistance of the underlying material is a function of $R_{sheet}$ , the distance between the contacts, L and the width of the contacts as shown in equation 5.6.

$$R_T = 2R_m + 2R_c + R_x \tag{5.5}$$

$$R_x = \frac{R_{sheet}L}{W} \tag{5.6}$$

The Resistance of the metal usually is very low ($R_c >> R_m$), therefore $R_m$ can be ignored. The equation then simplifies to that shown in equation 5.7.

$$R_T = \frac{R_{sheet}L}{W} + 2R_c \quad (5.7)$$

$R_{sheet}$ and $R_c$ can be evaluated by plotting the graph of $R_T$ versus L as shown in Figure 5.3.7(b). $R_{sheet}$ can be calculated by obtaining the gradient of the graph and $R_c$ by obtaining the intercept of the graphs. The ρ is obtained by dividing the sheet resistance by the film thickness, t as shown in equation 5.8.

$$\rho = \frac{R_{sheet}}{t} \quad (5.8)$$

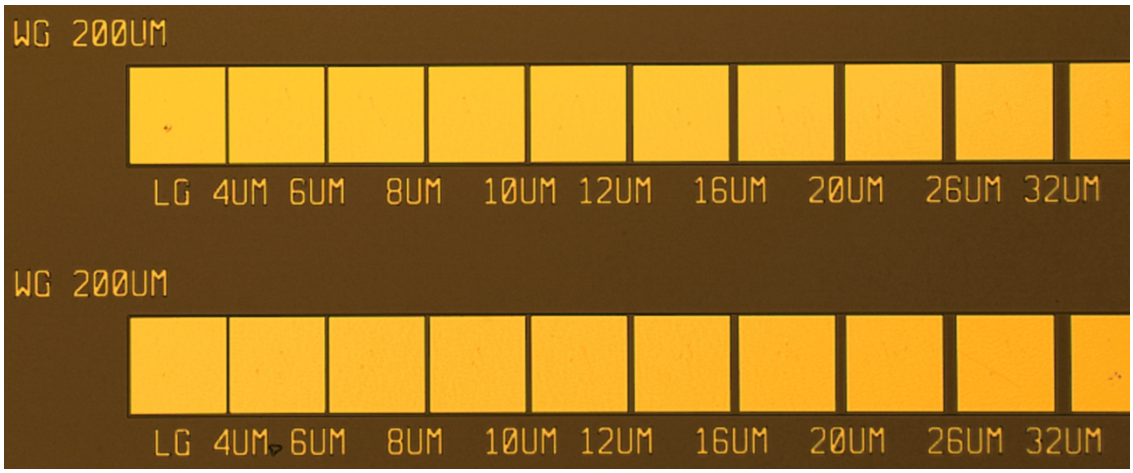


**Figure 5.3.7 (a): Linear TLM structures**

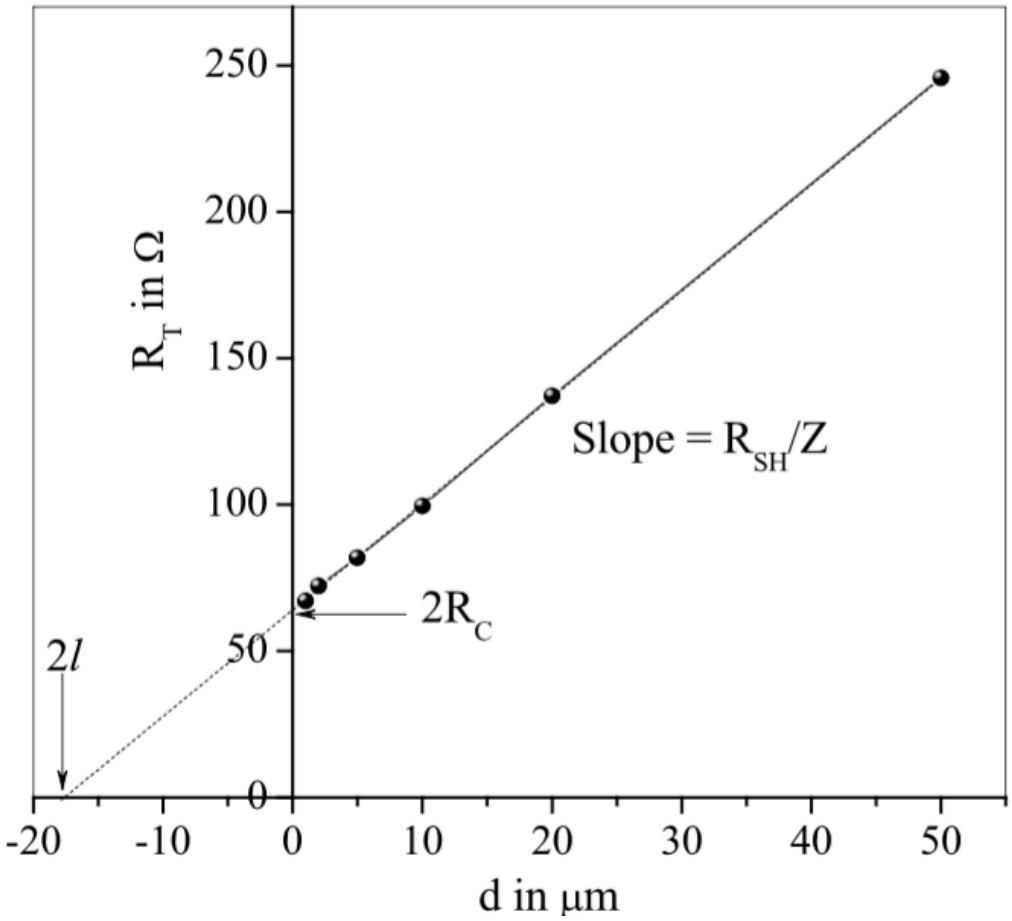


**Figure 5.3.7 (b): Total resistance measured versus distance between contacts [10].**

The chapter has described the characterisation and metrology techniques used in the research. Spectroscopic ellipsometry is used to give information regarding the thickness and refractive index of the film and x-ray photoelectron spectroscopy is used to identify the elements present in films and to obtain the band offsets between the dielectric and the semiconductor. The C-V based analysis of the films provide insight into the dielectric quality and the quality of the dielectric-semiconductor interface.

## 5.5 Reference

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# 6.“In-situ processing” of GaN MOSCAPs

## 6.1 Introduction

The impact of avoiding atmospheric exposure of the GaN surface on the electrical characteristics of GaN MOS capacitors is discussed in this chapter. This has been achieved by completing the MOCVD growth of GaN MOSCAP wafers with an in-situ deposited $SiN_x$ layer. A cluster tool with both etching and atomic layer deposition capability was used to process the samples “in-situ”. The in-situ deposited $SiN_x$ layer was first etched prior to samples being transferred under vacuum to the ALD reactor. The chapter also discusses the effect of various plasma pretreatments prior to the dielectric deposition in the ALD reactor and also the effect of a post gate metal annealing process using forming gas. The effect of the above in-situ processing, plasma pretreatments and post forming gas anneal (FGA) have been characterised by using capacitance-voltage and current voltage measurements.

## 6.2 Experimental procedure

The experiments used to evaluate the “in situ processing” of GaN MOSCAPs where the GaN surface is not subjected to atmospheric exposure were carried out on 15x15mm GaN samples diced from a 150 mm GaN on Si MOCVD grown wafer shown schematically in Figure 6.2.1(a). The layer structure was designed by collaborators at the Univeristy of Cambridge. The structure included a buffer layer to compensate for lattice mismatch between Si and GaN and a highly doped GaN layer was included for fabricating low resistance ohmic contacts. The key layers in the material structure were a 600 nm thick $1x10^{17}$ $cm^{-3}$ n-doped GaN layer which was capped with 5 nm $SiN_x$ as the final step in the wafer growth. Following dicing, the samples were prepared using a standard ultrasonic clean in acetone for 5 minutes before being rinsed in isopropropanol (IPA) and then in RO water. They were then processed in the cluster tool, using the chambers shown in Figure 6.2.2. The samples were first transferred to the etching chamber via the wafer handler where the $SiN_x$ was removed using a proven, low damage [1] reactive ion etching (RIE) process in an $SF_6$ plasma for 45 seconds at with an RF power of 50W, chamber pressure of

50mTorr and 50sccm $SF_6$ gas flow rate before being transferred under vacuum ($7.5x10^{-9}$ Torr) to the ALD chamber, where various plasma pretreatments were performed prior to the dielectric deposition. $Al_2O_3$ was chosen as the dielectric due to its favourable band offsets and high electric breakdown field[2][3]. 20nm thick $Al_2O_3$ films were deposited thermally using trimethyl aluminium (TMA) and $H_2O$ at $200^0$C.

The details of the various pretreatments used are listed in table 6.2.1. As reported in literature $N_2$ plasma has the capability to fill nitrogen vacancies and $H_2$ assists in removing carbon impurities [5]. Therefore, this work examines the effect of $N_2$ and $H_2$ plasma at different plasma powers and exposure times. A pretreatment with a combination of $N_2$ and $H_2$ was also examined using the plasma powers and times that gave the most favourable electrical data for each individual gas. In this process split, the sample was first exposed to the $H_2$ plasma followed by the $N_2$ plasma afterwards. No wet treatments have been carried out in this work to ensure the sample was always kept under vacuum and not affected by atmospheric exposure. MOS capacitor structures were fabricated on the samples after dielectric deposition. The capacitors contained 20nm Pt/ 200nm Au gate metal stack deposited on the $Al_2O_3$ dielectric using a shadow mask. These samples were then masked using photoresist to produce the ohmic contact to the highly doped GaN layer. Afterwards, 600nm of GaN was etched using $SiCl_4$ RIE at 8mTorr, 200W, 25 sccm. A 10nm Mo/40nm Al/20nm Mo/30nm Au ohmic contact was then deposited using E-beam evaporation and lifted off and was followed by another layer of lithography where contact to the ohmic metal was made by 20nm Ti/ 200nm Au that was also deposited ex-situ using E-beam evaporation. The exact details of the fabrication flow are shown in Appendix A. The MOS capacitors were then characterised electrically by measuring the C-V and I-V properties which are examined in detail in the following sections.

The samples with the most favourable electrical data were then subjected to a forming gas anneal ($H_2$ 10%: $N_2$ 90%) at $430^0$C for 30 minutes. The effect of the anneal on electrical properties on these samples are discussed in section 6.4.

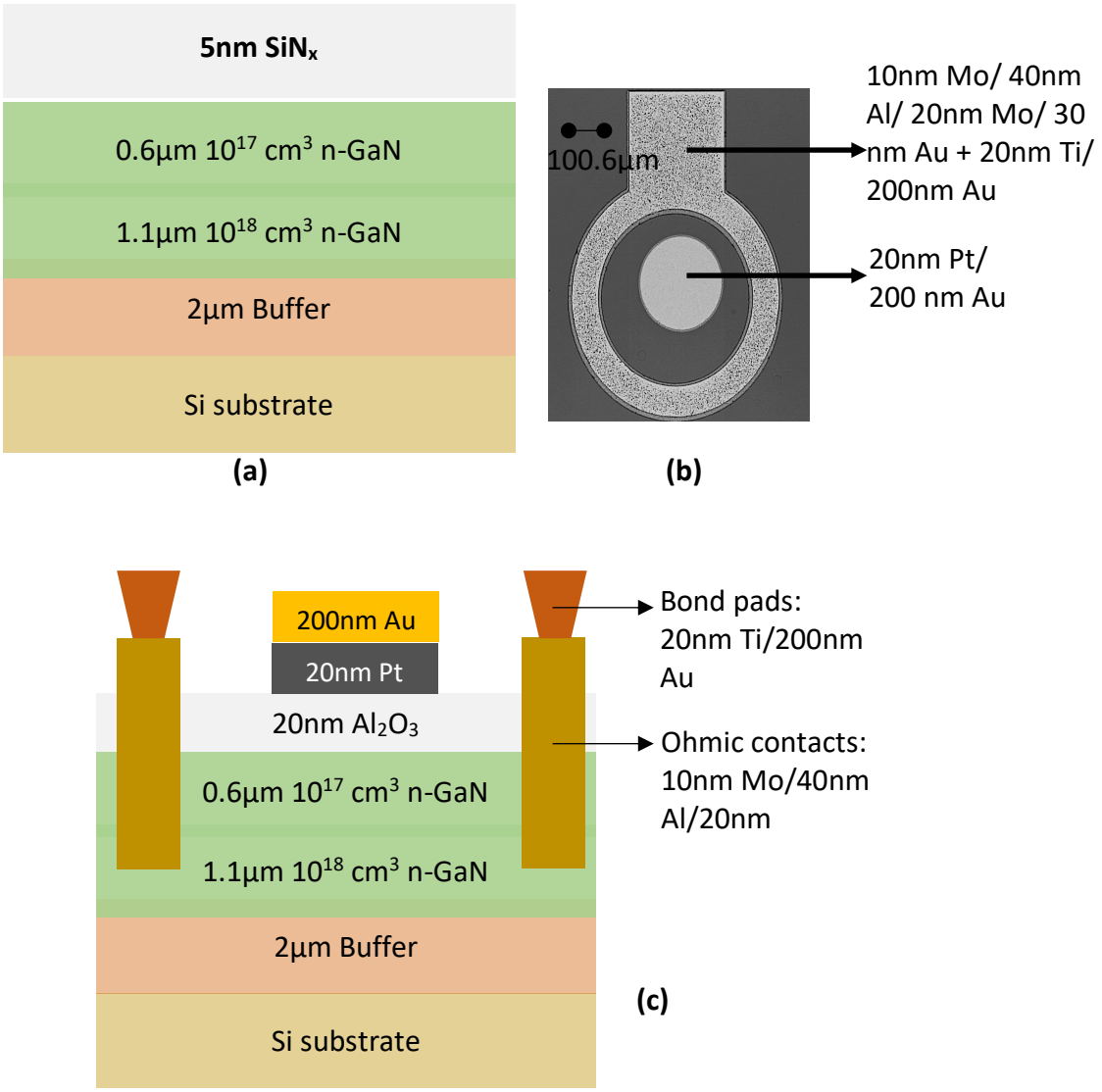



**Figure 6.2.1: (a) MOS capacitor layer structure (b) Fabricated MOS capacitor (c) Cross sectional view of fabricated MOS capacitor**

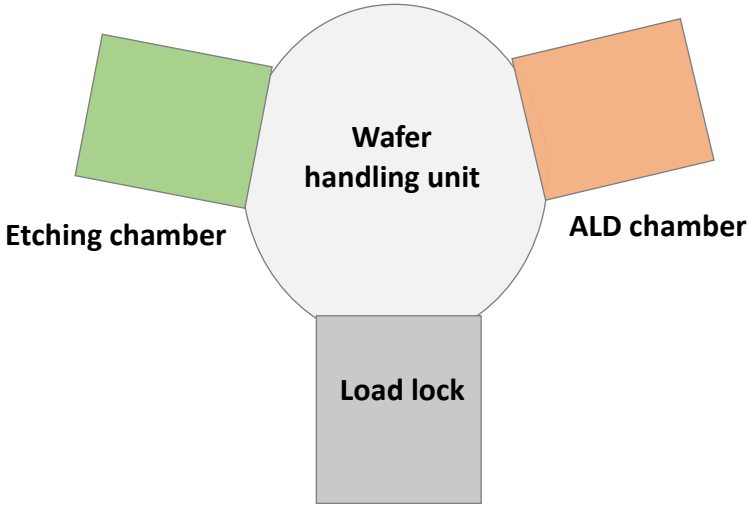



**Figure 6.2.2: Schematic of cluster tool**

| Plasma gas | Power/ (W) | Time/(minutes) |
|---|---|---|
| $N_2$ | 150 | 5 |
| $N_2$ | 300 | 5 |
| $N_2$ | 225 | 7 |
| $N_2$ | 75 | 7 |
| $N_2$ | 225 | 3 |
| $H_2$ | 200 | 5 |
| $H_2$ | 100 | 5 |
| $H_2$ | 150 | 3 |
| $H_2$ | 300 | 5 |

**Table 6.2.1: Summary of the pretreatments used**

## 6.3 Electrical Analysis: Pre FGA

This section examines the capacitance-voltage and current-voltage measurements at room temperature of the samples before various FGA processes . A summary of all the electrical data measured is represented in Table 6.3.1 and the graphical representations of all the data are attached in Appendix B. The following subsections discuss in detail the parameters in Table 6.3.1.

| Row | Plasma gas | Power (W) | Time (mins) | $\Delta_{Hysteresis}$ (mV) | $\Delta_{Dispersion}$ (mV) | $C_{acc}$ @1MHz ($\mu F/cm^2$) | $I_{leak}$ @1V ($A/cm^2$) | $V_{fb}$ (mV) | $V_{br}$ (V) |
|---|---|---|---|---|---|---|---|---|---|
| 1 | **SiN etch only** | **0** | **0** | **250** | **350** | **0.295** | **0.016** | -650 | **13.4** |
| 2 | $N_2$ | 75 | 7 | 350 | 350 | 0.313 | 0.018 | -550 | 10.5 |
| 3 | **$N_2$** | **150** | **5** | **200** | **250** | **0.323** | **0.015** | -650 | **14.4** |
| 4 | $N_2$ | 225 | 7 | 300 | 400 | 0.312 | 0.0254 | -550 | 10.7 |
| 5 | $H_2$ | 100 | 5 | 400 | 350 | 0.264 | 0.0651 | -100 | 12.6 |
| 6 | **$H_2$** | **150** | **3** | **150** | **200** | **0.288** | **0.0142** | -250 | **13.6** |
| 7 | $H_2$ | 200 | 5 | 400 | 250 | 0.294 | 0.0187 | -500 | 13.4 |
| 8 | $H_2$ +$N_2$ | 150 +150 | 3 + 5 | 300 | 350 | 0.323 | 0.058 | -350 | 12.6 |

**Table 6.3.1: Summary of electrical data obtained for various pretreatments, $\Delta_{Hysteresis}$= C-V hysteresis, $\Delta_{Dispersion}$= frequency dispersion, $C_{acc}$= accumulated capacitance, $I_{leak}$= leakage current, $V_{br}$= breakdown voltage**

**C-V hysteresis**

The room temperature C-V hysteresis evaluation, measured at a frequency of 1 MHz, comprised of a forward voltage sweep from -5v to +5V and back to -5V. This enabled the determination of the flat band voltage hysteresis, $\Delta V_{Hysteresis}$, between the forward and backward sweeps. A maximum voltage of 5V was applied because it is the applied voltage to the gate of the envisioned final transistors, while a minimum of -5V was chosen to ensure sufficient voltage is applied for the C-V to show depletion characteristics.

It can be observed that the sample with no pretreatment post the $SiN_x$ etch (Row 1 in Table 6.3.1) produced a hysteresis of 250mV. The exposure to an $N_2$ plasma at 75W for 7 minutes post etch (Row 2) increased the hysteresis to 350mV. Increasing the power to 225W (Row 4) resulted in a hysteresis of 300mV, which is still higher than the sample with no pretreatment. However, with a $N_2$ plasma power of 150W and decreasing the exposure time to 5 minutes resulted in a 200mV hysteresis (Row 3). The $N_2$ 150W 5 minute plasma therefore assisted in reducing interface traps and produced the lowest hysteresis compared to the other $N_2$ plasma treated samples

Three different hydrogen plasma pretreatments were also examined; 100W for 5 minutes, 200W for 5 minutes and 150W for 3 minutes. In comparison to the samples that had no pre-treatments (Row 1 of Table 6.3.1), the hysteresis increased to 400mV when a 100W, 5 minute $H_2$ plasma was used (Row 5) and the hysteresis remained at 400mV when the power was doubled to 200W (Row 7). However, a power of 150W and an exposure time of 3 minutes reduced the hysteresis to 150mV. In comparison to all the pretreatments of this study, $H_2$ plasma pretreatment at 150W for 3 minutes produced the lowest hysteresis. Figure 6.3.1 shows the $\Delta V_{Hysteresis}$ data of the sample that had no pretreatments after the $SiN_x$ etch, and the sample that produced the lowest $\Delta V_{Hysteresis}$ from the $N_2$ plasma treatment and the $H_2$ plasma treatment.

The $H_2$ pretreatment at 150W for 3 minutes and $N_2$ pretreatment at 150W for 5 minutes plasma were then both used to check the effect of a combined treatment. The sample was first exposed to the $H_2$ plasma and then to the $N_2$ plasma. However, this resulted in a hysteresis of 300mV (Row 8 of Table 6.3.1), which was again much higher than the untreated samples.

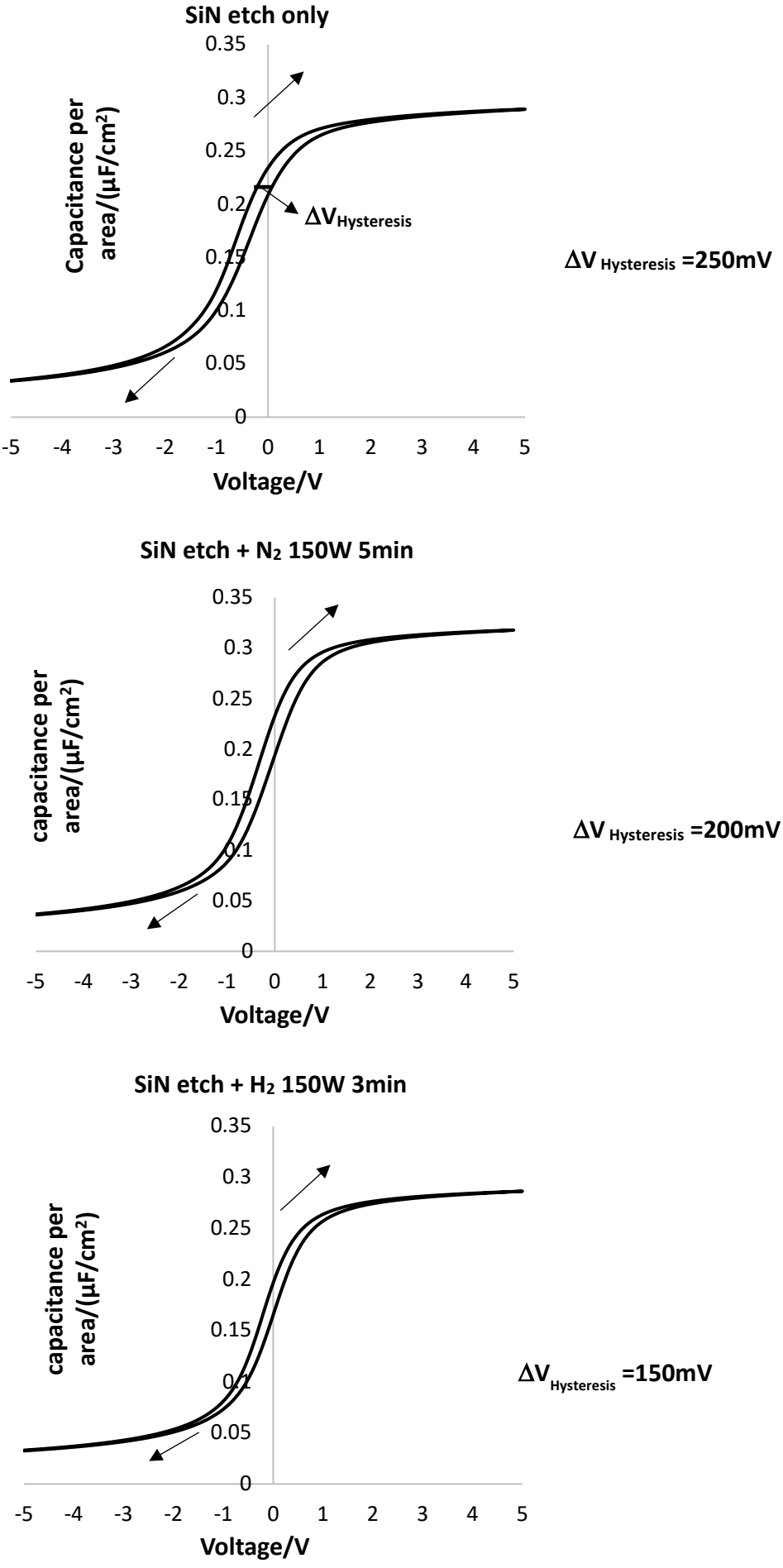


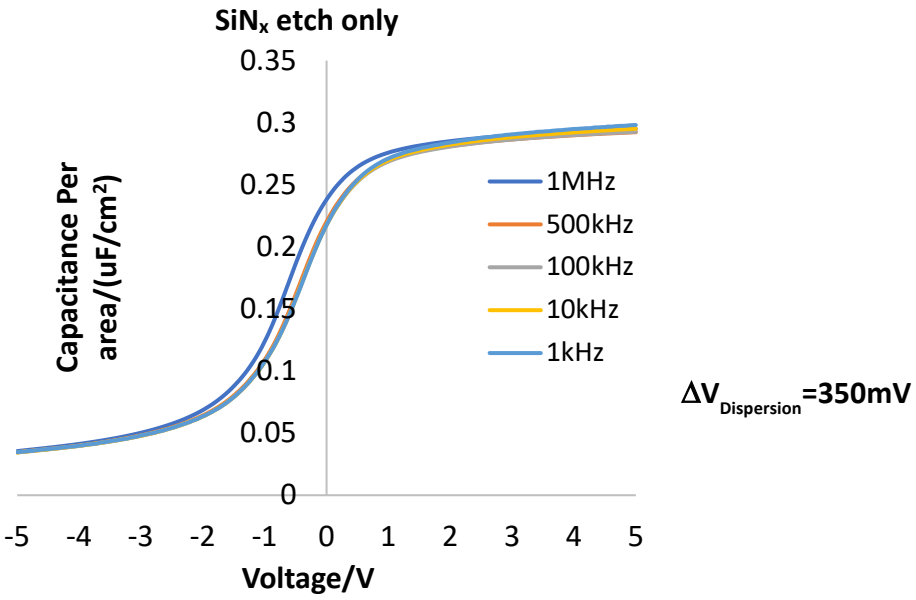

**Figure 6.3.1: C-V hysteresis characteristics measured at 1MHz**

**Frequency Dispersion**

In order to calculate the frequency dispersion, $\Delta_{Dispersion}$ the capacitance response was measured at frequencies ranging from 1MHz to 1kHz. Frequency dispersion was calculated by measuring the maximum difference in the flat band voltage across this range of frequencies as discussed previously.

Similar trends to the C-V hysteresis were also observed for the frequency dispersion, where the 5 minute, 150W $N_2$ 150W (Row 3 of Table 6.3.1) 3 minute, 150 W $H_2$ (Row 6) plasma treatments produced the lowest $\Delta_{Dispersion}$ of 250 mV and 200 mV respectively. These results are shown in Figure 6.3.2 along with the sample that had no pretreatments, which had frequency dispersion of 350mV.

The combination of both $N_2$ and $H_2$ plasma resulted again in degraded performance with a higher frequency dispersion of 350mV (Row 8 of Table 6.3.1).



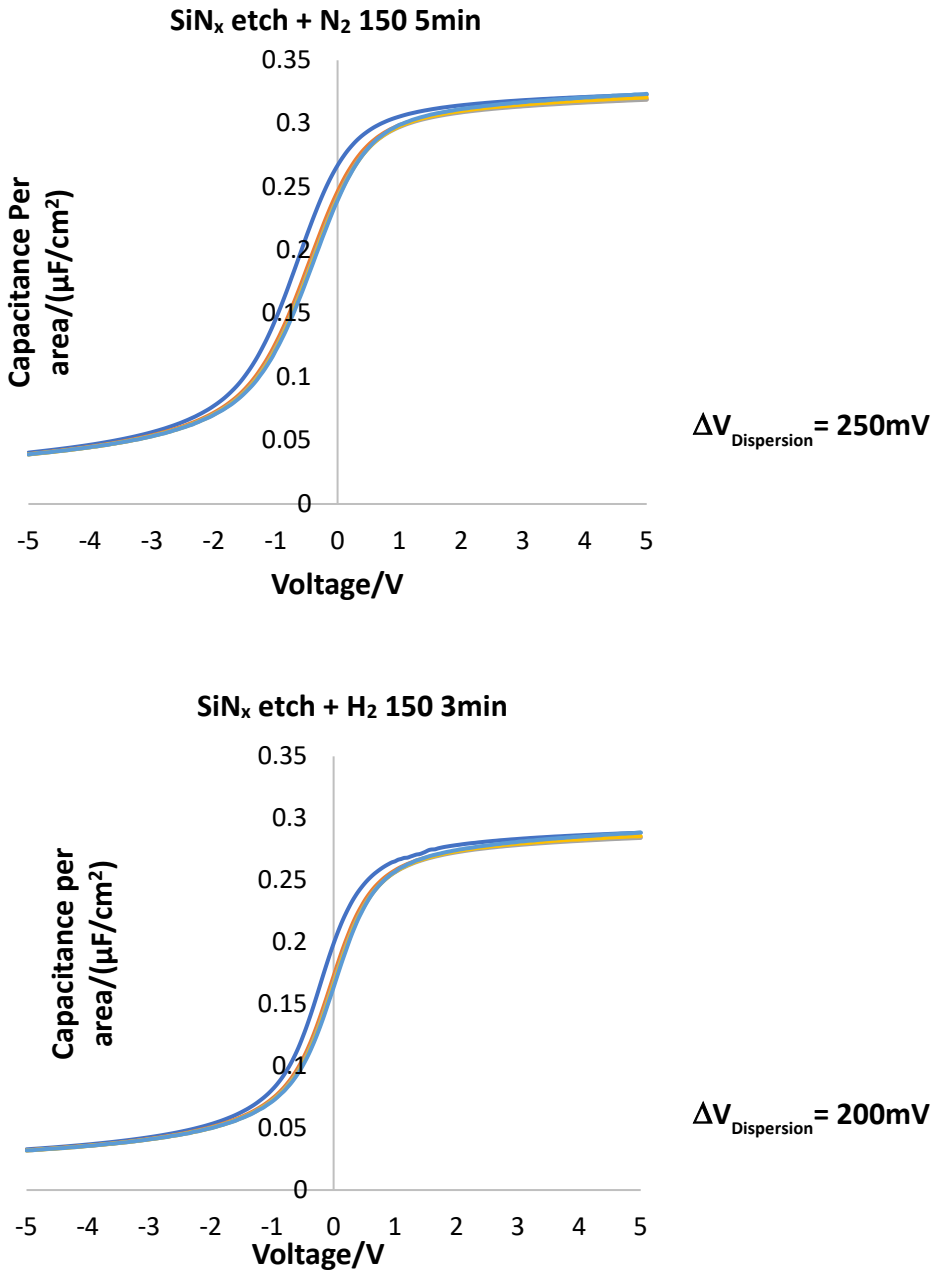



**Figure 6.3.2: Frequency dispersion characteristics for the pretreatments used**

**Leakage and breakdown**

The leakage current through the dielectric, $I_{leak}$ and breakdown voltage, $V_{br}$ data of the various pretreated samples are depicted in Figure 6.3.3 The exact values for leakage current at 1V and breakdown voltage are shown in Table 6.3.1. The lowest leakage current values are also obtained for the sample that had an $H_2$ plasma pre-treatment at 150W for 3 minutes, this is followed by the sample with an $N_2$ plasma pre-treatment at 150W for 5 minutes and the sample that had no pre-treatments.

The highest breakdown voltage of 14.4 V was achieved for the film that had an $N_2$ 150W 5 minutes plasma pretreatment prior to the dielectric deposition, this was then followed by

the $H_2$ 150W 3minutes plasma with a $V_{br}$ of 13.6 V and the samples that had only the $SiN_x$ etch with no pretreatment with a $V_{br}$ of 13.4V.

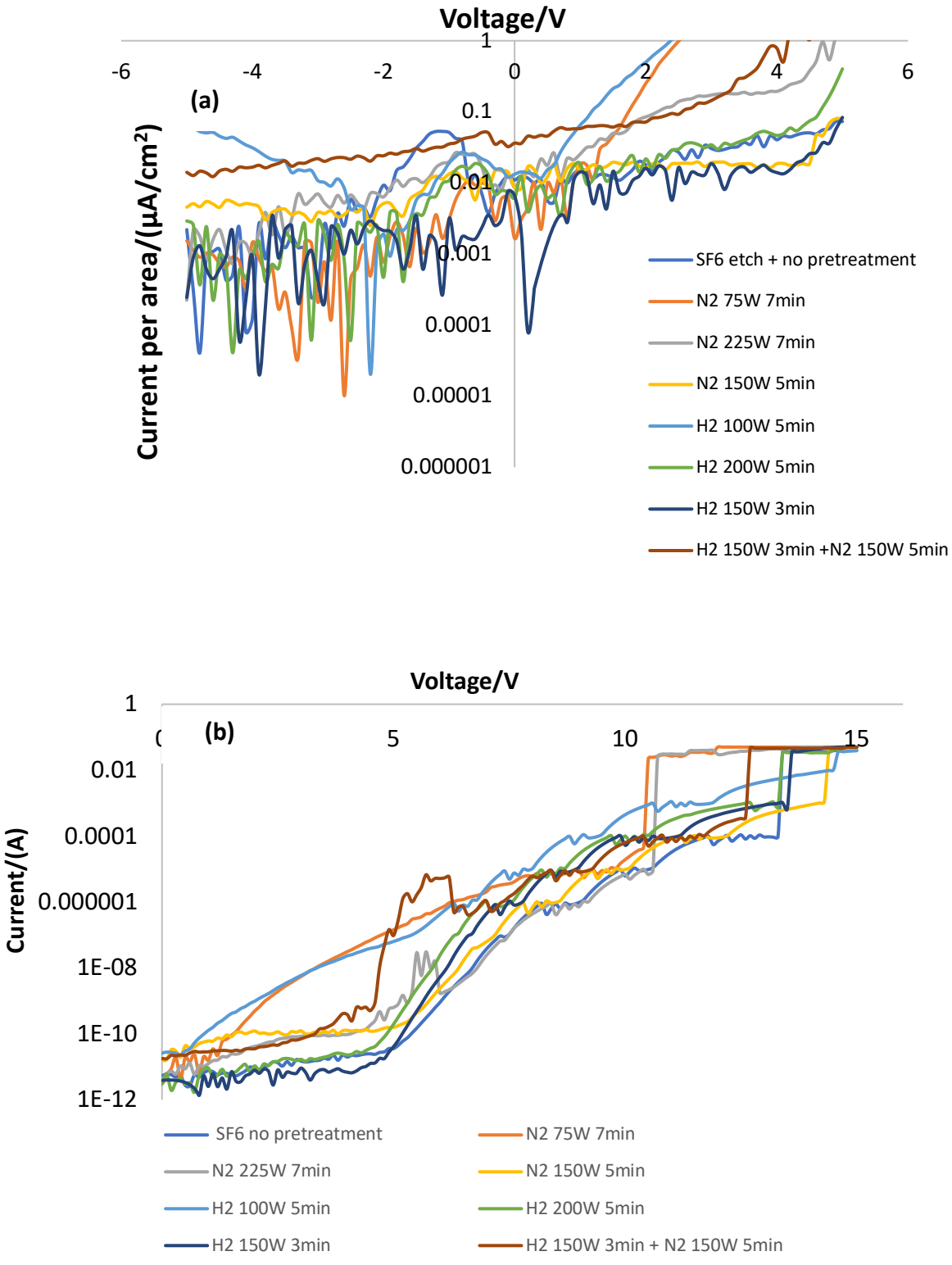



**Figure 6.3.3: Effect on (a) leakage current and (b)breakdown voltage of the various pretreatments**

Similar trends are seen for both the $H_2$ and $N_2$ plasma treatments, where decreasing the power below 150W and increasing the power above 150W resulted in higher $\Delta_{Hysteresis,}$ $\Delta_{Dispersion}$ and leakage current. This could be because the high plasma power induces damage to the GaN surface, while at low power there isn't sufficient energy for the atomic species in the plasma to interact with the surface. Compared to the sample that had no pre-treatments after the $SiN_x$ etch, $N_2$ and $H_2$ plasma treatments have resulted in a reduction in both $\Delta_{Hysteresis}$ and $\Delta_{Dispersion}$ and improvements to the leakage current and breakdown voltage.

It should also be noted that that the accumulation capacitance attained is lower than the theoretical capacitance of 0.403µF/cm$^2$ for 20nm $Al_2O_3$, calculated using a relative permittivity, $\varepsilon_r$ of 9.1[3]. Based on the measured accumulation capacitance, and assuming the $Al_2O_3$ layers are 20 nm thick, the relative permittivity of the films deposited are between 6.6 and 7.3. The highest $\varepsilon_r$ obtained was from the film deposited on the GaN surface that had been exposed to the optimal $N_2$ plasma pretreatment. Further, the breakdown field achieved for the samples that had the best electrical data in terms of capacitance related metrics were between 6.7-7MV/cm, which is also lower than that achieved in literature of 9MV/cm [6]. The lower breakdown voltage could be a result of possible carbon impurities present in the films [7].

It is evident from the results that the $N_2$ and $H_2$ plasma pretreatments assisted in enhancing the GaN-$Al_2O_3$ interface. The results summarised in Table 6.3.1 indicate that the samples that that gave the best electrical characteristics were: the sample which had no pretreatments after the SiNx etch, the sample which had $N_2$ pretreatment at 150W for 5 minutes and the sample which had $H_2$ pretreatment at 150W for 3 minutes. The following section investigates the effect of a forming gas anneal (FGA) on these samples.

# 6.4 Electrical analysis: Post FGA

The selected samples from the previous section with the best performance in regards to CV hysteresis, frequency dispersion, leakage current, and breakdown voltage were subjected to a 430$^0$C forming gas anneal for 30 minutes after the fabrication of the full MOS capacitor. This section examines the effect of an FGA on the electrical characteristics of the

MOS capacitors and a summary of all the electrical data measured are represented in Table 6.4.1

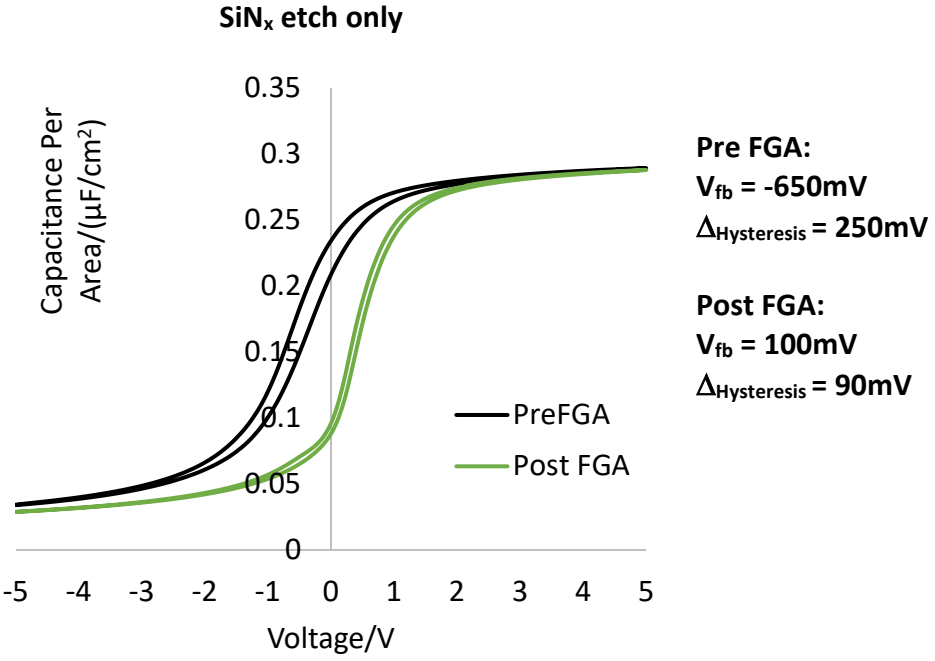
| Plasma gas | Power (W) | Time (minutes) | $\Delta_{Hysteresis}$ (mV) | $\Delta_{Dispersion}$ (mV) | $C_{acc}$ @1MHz ($\mu F/cm^2$) | $I_{leak}$ @1V ($A/cm^2$) | $V_{br}$ (V) |
|---|---|---|---|---|---|---|---|
| SiN etch only | 0 | 0 | 90 | 150 | 0.285 | 0.0152 | 15 |
| $N_2$ | 150 | 5 | 60 | 50 | 0.320 | 0.0148 | 14.2 |
| $H_2$ | 150 | 3 | 70 | 60 | 0.296 | 0.0132 | 14.2 |

**Table 6.4.1: Summary electrical data obtained post FGA**

**C-V hysteresis**

Figure 6.4.1 depicts the C-V hysteresis of pre and post FGA for the selected samples. All the samples demonstrated greater than a 50% reduction in hysteresis post FGA. A 64% reduction for the samples that had no pretreatment after the $SiN_x$ etch was measured, as well as a 70% reduction for $N_2$ treated samples and a 60% reduction for $H_2$ treated samples. Post FGA, the sample that was exposed to an $N_2$ plasma pre-treatment after the $SiN_x$ etch produced the lowest hysteresis of 60mV.

It can also be observed from Figure 6.4.1 that the C-V curves have also shifted towards the positive direction after FGA. This shift could be a consequence of the reduction in fixed positive charge of the oxide due to the FGA and this will be discussed further in the discussions section.



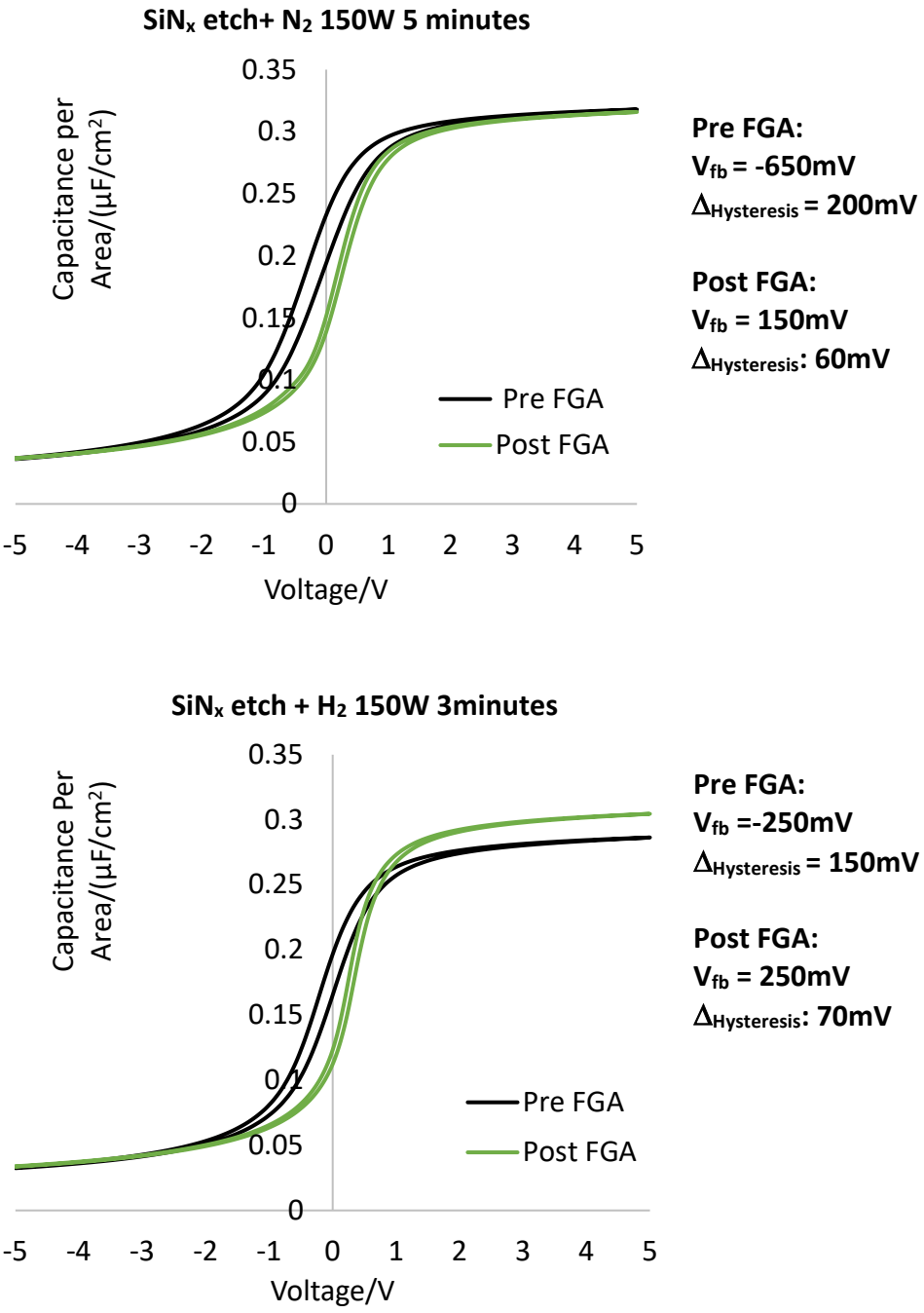


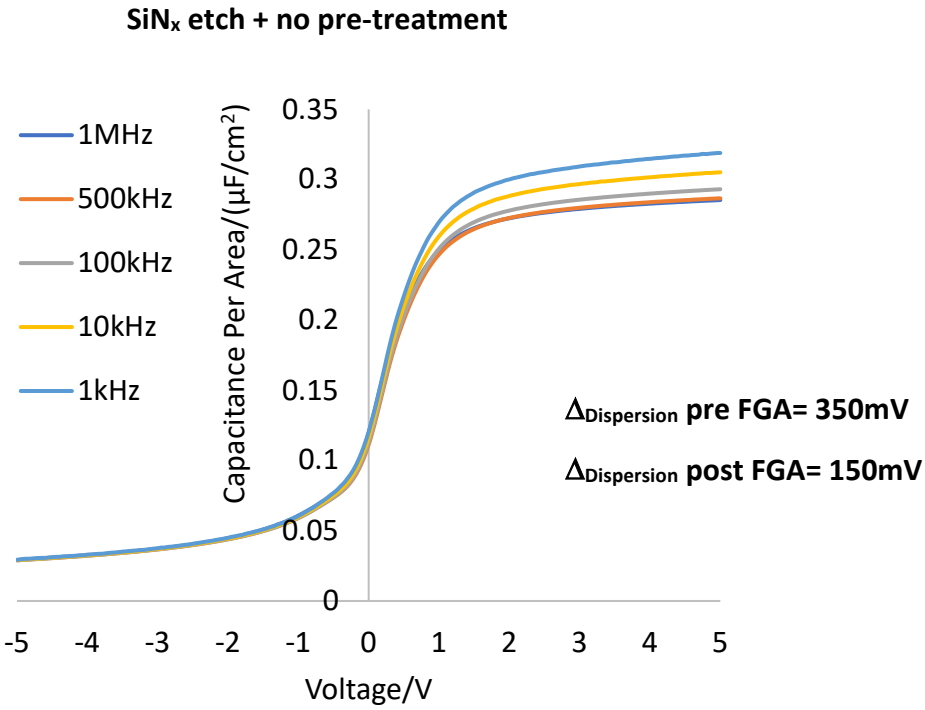

**Figure 6.4.1: Effect of FGA on C-V hysteresis**

**Frequency dispersion**

Figure 6.4.2 depicts the C-V curves of the optimally $N_2$ and $H_2$ plasma pretreated samples and the sample that only went through the $SiN_x$ etch measured at different frequencies. It can be observed that the FGA has also assisted in reducing the frequency dispersion. The dispersion in the sample with no plasma pretreatment has reduced from 350 to 150mV (57.1% reduction). There has been a reduction from 200 to 60mV for samples with $H_2$

plasma exposure (70% reduction), and a reduction from 250 to 50mV for the samples with with $N_2$ plasma (80% reduction). The $N_2$ plasma pretreatment has therefore resulted in the lowest frequency dispersion after FGA.

Shown in Figure 6.4.3 is the accumulation capacitance determined at different frequencies for $N_2$ pretreatment, $H_2$ pretreatment, and no pretreatment. A variation of 1.25% and 0.33% was observed in the accumulation capacitance for the $H_2$ and the $N_2$ treated samples. However, the sample with no pretreatment shows a variation of 13.7% in the accumulated capacitance. This variation is most likely a result of the presence of border traps in the oxide. Therefore, it appears that the pretreatments have assisted in reducing the border trap density.



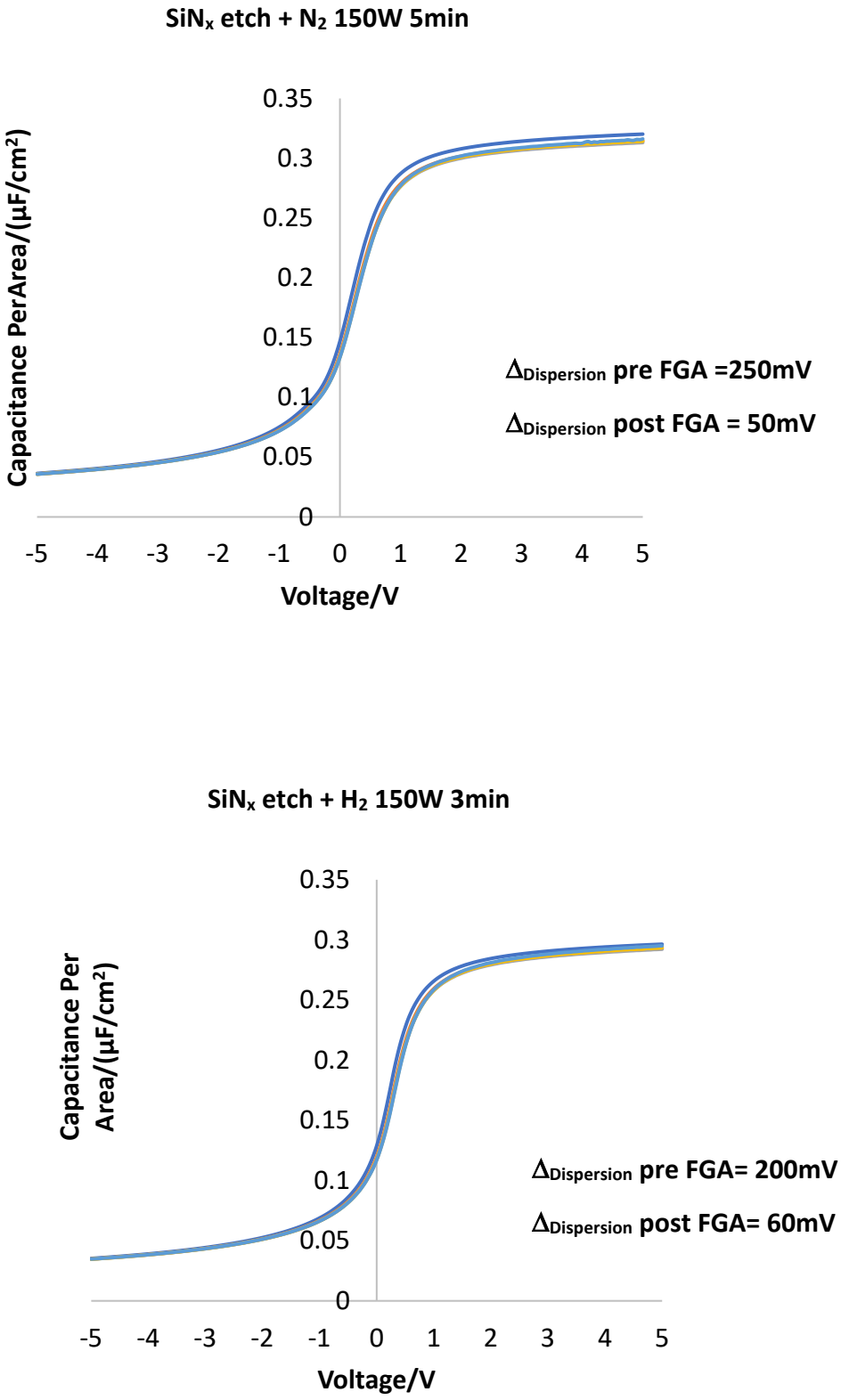



**Figure 6.4.2: Effect of FGA on frequency dispersion**

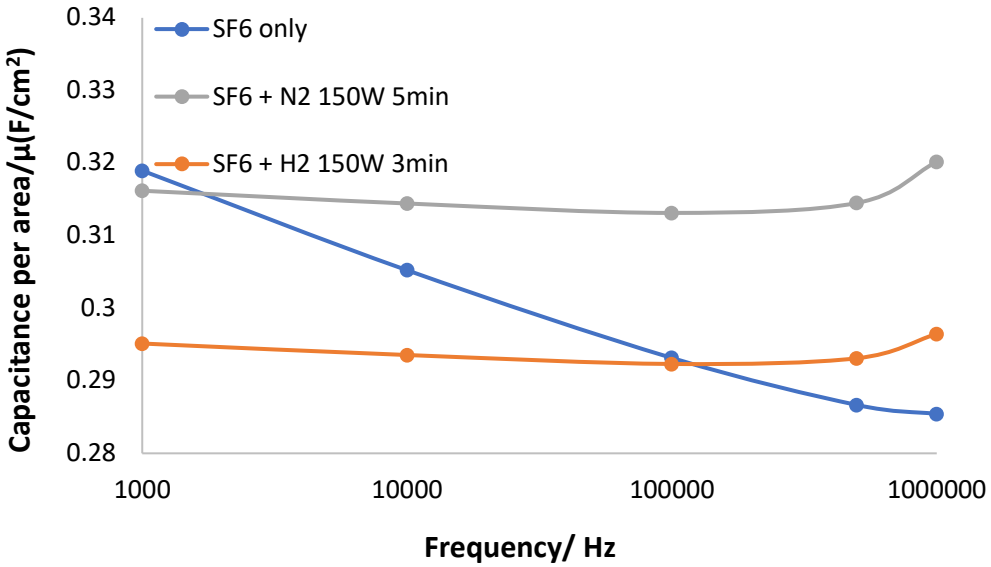



**Figure 6.4.3: Accumulation capacitance and different frequencies**

**Stress voltage measurements**

Figure 6.4.4 illustrates the stress voltage measurements of the optimally $N_2$ and $H_2$ plasma pretreated samples, as well as the sample with no pretreatment. These were measured at 10kHz, while varying the range of voltage from -5 to 0V and back to -5V then -5 to 1V and back to -5V and so on. The x-axis values denote the final voltage value to which the voltage was swept. It can be seen that the change in the hysteresis measured from $N_2$ plasma pretreatment was the lowest pre FGA. However, after the samples were annealed the hysteresis measured at the different voltage ranges remained the same for all the samples. No hysteresis was measured until the voltage range reached 5 V. Over this bias range, the hysteresis measured was 50mV, which is still less than the values obtained pre FGA.

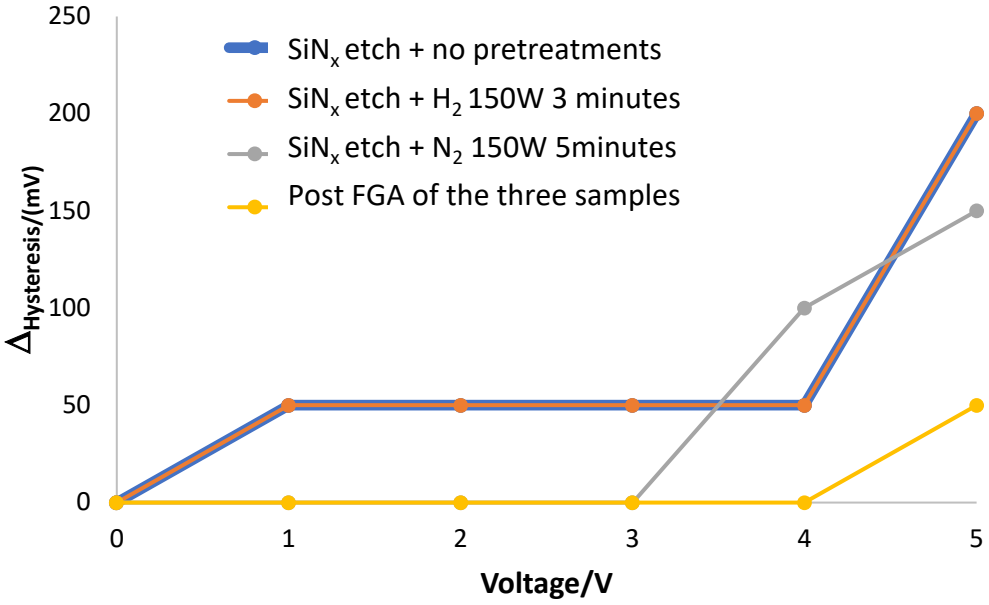



**Figure 6.4.4: Effect of pretreatments and FGA on stress voltage measurements**

**C-V slope**

The differentiation of the C-V curves of the samples pre and post FGA are depicted in Figure 6.4.5. The derivative can be used to give an indication of the interface trap density between the semiconductor and oxide. The higher the slope the lower interface trap density. The FGA has resulted in an increase in the C-V slope. The anneal has therefore assisted in reducing the number of interface traps

Pre FGA, the C-V slopes of all samples were in the range 0.10-0.16 µF/cm$^2$V. This increased to values between 0.20 and 0.23 µF/cm$^2$V after FGA, with the sample exposed to the optimal $H_2$ plasma pretreatment again having the highest slope, and therefore the lowest number of interface traps.

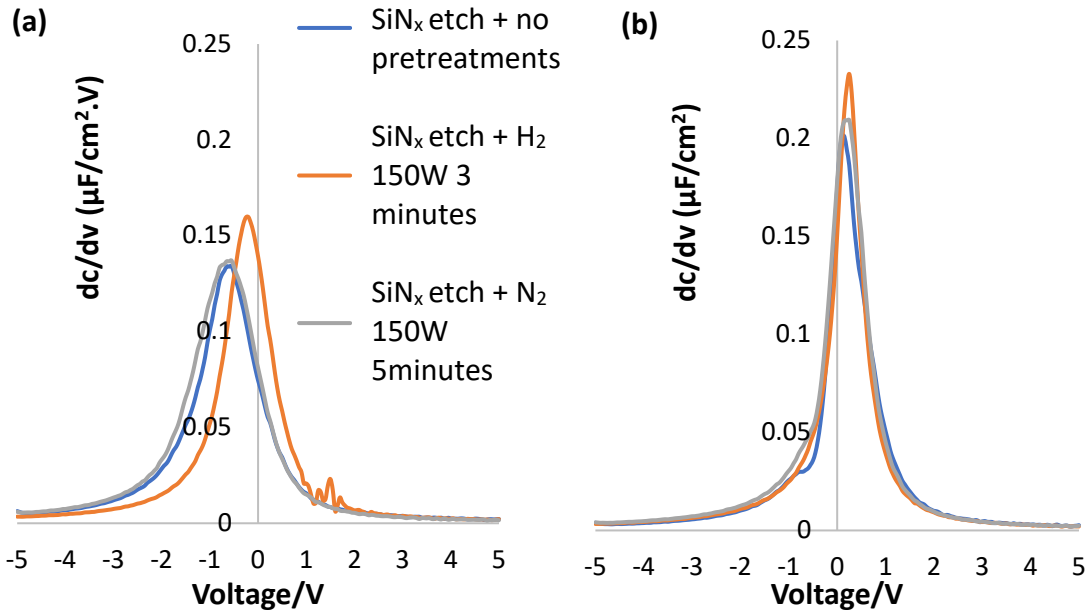
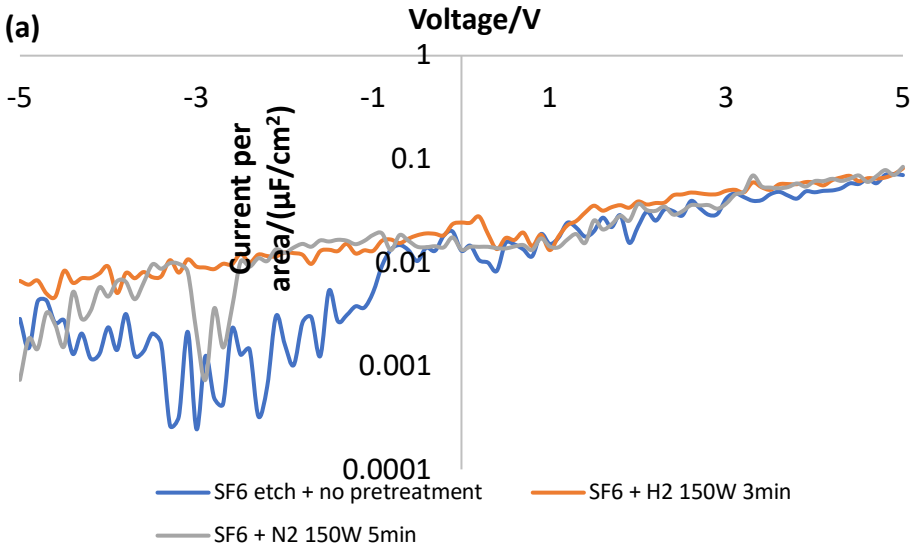



**Figure 6.4.5: Differentiation of the C-V curve (a) pre and (b) post FGA**

**Leakage and breakdown**

The leakage current and breakdown voltage of samples after FGA are shown in Figure 6.4.6. The lowest leakage current is obtained for the films that had an $H_2$ plasma pretreatment for 3 minutes. However, the breakdown voltage is the highest (15V) for the samples that had no pre-treatments. The films with the optimal $N_2$ and $H_2$ plasma pretreatments both have breakdown voltage of 14.2V after FGA.



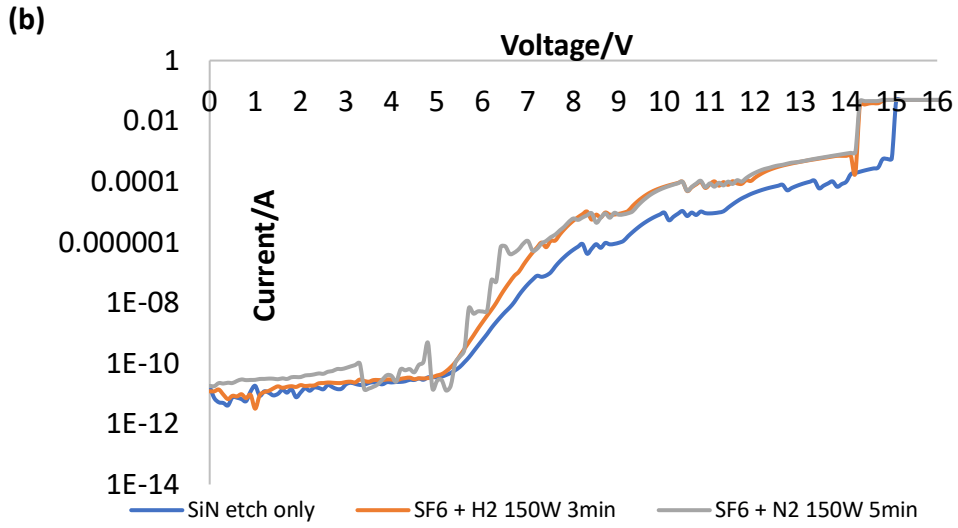



**Figure 6.4.6: (a)Leakage and (b)breakdown characteristics of the annealed films**

**Discussion**

Table 6.4.2 summarises the electrical data obtained for the optimally $N_2$ and $H_2$ plasma pretreated samples and the samples with no pretreatment pre and post FGA. It can be observed that the FGA has made significant improvements to the electrical properties of the samples. C-V hysteresis has reduced by 64% for the sample with no pretreatments, while it has reduced by 53% for the $H_2$ treated sample and by 70% for the $N_2$ treated sample. The frequency dispersion has reduced by 57% for the sample with no pretreatment, by 70% for the $H_2$ treated sample and by 76% for the $N_2$ treated sample. A $\Delta_{Hysteresis}$ of 250mV and a $\Delta_{Dispersion}$ 310mV was reported for GaN -$Al_2O_3$ MOS capacitors that had no pretreatment but underwent a post FGA at 430$^0$C for 30 minutes [8]. Therefore, it can be concluded that the in-situ $SiN_x$ capped layer, has effectuated a reduction of 64% in the $\Delta_{Hysteresis}$ and a reduction of 51.6% in $\Delta_{Dispersion}$.

Considerable improvements have also been made to the slope of the C-V curve post FGA, indicating further the improvement to the GaN-$Al_2O_3$ interface. Table 6.4.2 also shows the fixed charge in the films, which has been calculated using equation 6.1. The equation assumes is no trapped charge present in the oxide. The difference between $\Phi_{ms}$ and the measured flat band voltage, $V_{fb\ measured}$ multiplied by the accumulated capacitance per area produces the charge density. $\Phi_{ms}$ is calculated using theoretical values reported in literature. It can be observed from Table 6.4.2 that initially, a positive fixed charge existed in the $Al_2O_3$ films and the FGA has reduced this. This indicates that the FGA may have the

effect of passivating unsatisfied positive bonds in the oxide [9]. Similar results are also obtained in literature where an FGA assists in reducing the fixed positive charge in $Al_2O_3$ films [9].

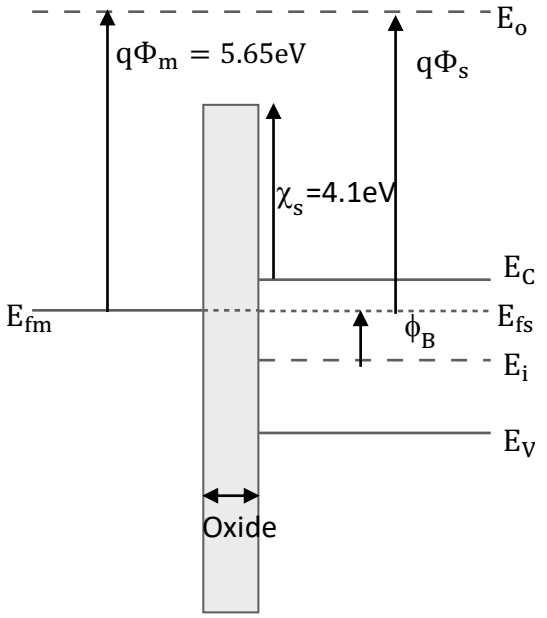
Figure 6.4.7 illustrates the ideal band diagram of the GaN MOS capacitor system, with Pt as the metal electrode and $Al_2O_3$ as the dielectric. The ideal $V_{fb}$ voltage in the absence of any fixed charge has been calculated to be -630mV using equation 6.2. Details of the calculation are depicted on the right-hand side of Figure 6.4.7. The $V_{fb}$ values measured from the samples post FGA are indeed different from the calculated values. This could be as a result of the dissimilarity between the idea and actual work function of platinum deposited and the presence of fixed charge in the oxide.

The leakage current too has reduced but not significantly (<10%) as a result of the FGA process. A slight improvement in the breakdown voltage is observed for the sample that had no plasma pretreatments post $SiN_x$ etch and the hydrogen treated samples, however for the samples that had the $N_2$ plasma pretreatment no significant change was observed.

$$Q_f = (\Phi_{ms} - V_{fb_{measured}})C_{ox} \text{ [10]} \qquad 6.1$$

$$V_{fb} = \Phi_{ms} - \frac{Q_{pol}}{C_{ox}} = -0.630V \qquad 6.2$$

$Q_{pol}$= Polarisation charge= -0.29 x $10^{-6}$ C [11].




$\Phi_m = \Phi_{Pt} = 5.65eV$[12]

$\chi_s = 4.1eV$[11]

$\Phi_s = \chi_s + (\frac{E_g}{2} - \phi_B)$

$\phi_B = -\frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right)$

$\phi_B \approx 0.06$

$\Phi_s = 4.1 + (1.7 - 0.06) = 5.74eV$

$\Phi_{ms} = \Phi_m - \Phi_s = -0.09eV$

**Figure 6.4.7: Band data and calculation of ideal $V_{fb}$**

| | | $SiN_x$ etch only | $SiN_x$ etch + $H_2$ 150W 3 minutes | $SiN_x$ etch + $N_2$ 150W 5 minutes |
|---|---|---|---|---|
| **Pre FGA** | $V_{flatband}$/(mV) | -650 | -250 | -650 |
| | $\Delta_{hysteresis}$/mV | 250 | 150 | 200 |
| | $\Delta_{Dispersion}$/mV | 350 | 200 | 250 |
| | $C_{acc}/(\mu F/cm^2)$ | 0.295 | 0.288 | 0.323 |
| | $\varepsilon_r$ | 6.67 | 6.5 | 7.3 |
| | $(dC/dV)/(\mu F/cm^2.V)$ | 0.134 | 0.160 | 0.137 |
| | $I_{leak}/(\mu A/cm^2)$ at 1V | 0.016 | 0.0151 | 0.0142 |
| | $V_{br}$/(V) | 13.4 | 13.6 | 14.4 |
| | $Q_f/cm^2$ | $1x10^{12}$ | $2.88x10^{11}$ | $2.88x10^{12}$ |
| | | | | |
| **Post FGA** | $V_{flatband}$/(mV) | 100 | 250 | 150 |
| | $\Delta_{hysteresis}$/mV | 90 | 70 | 60 |
| | $\Delta_{Dispersion}$/mV | 150 | 60 | 60 |
| | $C_{acc}/(\mu F/cm^2)$ | 0.285 | 0.296 | 0.320 |
| | $\varepsilon_r$ | 6.64 | 6.69 | 7.23 |
| | $(dC/dV)/(\mu F/cm^2.V)$ | 0.201 | 0.215 | 0.209 |
| | $I_{leak}/(\mu A/cm^2)$ at 1V | 0.0152 | 0.0132 | 0.0148 |
| | $V_{br}$/(V) | 15 | 14.2 | 14.2 |
| | $Q_f/cm^2$ | $-3.4x10^{11}$ | $-6.29x10^{11}$ | $-4.8x10^{11}$ |

**Table 6.4.2: Summary of pre and post FGA**

# 6.5 Summary

This chapter has discussed a route to the realisation of GaN MOS-capacitors (MOSCAPs) which avoids air exposure of the GaN surface by utilising in-situ deposition of $SiN_x$ as the final part of substrate growth. A clustered plasma etch and atomic layer deposition (ALD) tool has then been used to etch the $SiN_x$ cap and transfer under vacuum to the ALD chamber where surface pretreatments and dielectric growth is performed.

The effect of $N_2$ and $H_2$ plasma pretreatments after the $SiN_x$ etch were also investigated. $N_2$ 150w for 5 minutes and $H_2$ 150W for 3 minutes produced the best electrical data and indicated reduction in interface traps. These optimally plasma pretreated samples along

with the sample that had no plasma pretreatments were then subjected to an FGA at $430^0$C for 30 minutes. The $\Delta_{Hysteresis}$ of 90mV and $\Delta_{Dispersion}$ of 150mV achieved from the samples were much lower than the reported values of 250mV and 350mV of untreated GaN-$Al_2O_3$ MOS capacitors that have undergone similar thermal treatment [7]. This confirms the importance of a GaN surface that is unexposed the atmosphere.

Significant reduction in the interface traps and positive fixed charge were observed for all of the samples after the FGA. These reductions are encouraging for the realisation of high power GaN devices. The breakdown voltage of the films was however still lower than reported values. This may be due to the contaminants such as carbon present in the ALD films, and emphasises that the quality of the film still needs to be improved.

# 6.6 Reference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# 7. Atomic layer deposition and characterisation of aluminium nitride

## 7.1 Introduction

It has been reported that as a consequence of depositing $Al_2O_3$ on GaN, a $GaO_x$ suboxide is formed at the GaN-$Al_2O_3$ interface. Ga-O bonds have proven to increase interface states, which are undesirable in devices due to increased trapping [1]. Further, the $GaO_x$ suboxides are not lattice matched to that of GaN unlike AlN. The AlN also prevents the formation of an oxide layer and hence provides a better interface with GaN. There are various chemistries of growing AlN reported in literature. These include TMA with $N_2$, TMA with $NH_3$ and TMA with $N_2$ and $H_2$ [2][3]. The reaction with $NH_3$ of which are shown below:

$$Al(CH_3)_2 + NH_3 \longrightarrow AlN + 3CH_4$$

The main impurity observed in these chemistries has been carbon. ALD reactions using only $N_2$ have shown a higher content of carbon when compared to those using $NH_3$ and $N_2$ and $H_2$ plasma [2]. In this work a mixture of $N_2$ and $H_2$ plasma gas was used because the gas flow ratios can be controlled separately. The two main factors that affects the purity of the film have been the plasma exposure time and hydrogen flow rate. Low plasma exposure times resulted in chemically non-inert films while low flow rates resulted in insufficient removal of the alkyl group.

This chapter illustrates the effect of inserting an aluminium nitride (AlN) interlayer between GaN and an ALD deposited $Al_2O_3$ dielectric film. The AlN film has been deposited using plasma ALD with trimethylaluminium (TMA) and a mixed $N_2$ and $H_2$ plasma. To this end, the effect of varying the process parameters on growth rate and refractive index were examined and the respective ALD windows were identified. These films were initially grown on silicon and the process conditions that gave the most favourable results were used as deposition conditions on GaN MOS capacitors shown in Figure 7.2.1(a)(i). The films were analysed chemically on GaN using XPS and electrically by performing C-V and I-V

measurements. Electrical data of 4nm and 2nm AlN interlayers were initially examined and the most favourable of the two processes was then transferred on to samples shown in Figure 7.2.1a(ii) that went through an in-situ SiN etch and ALD process. The experimental details of the processes are provided in the following section.

## 7.2 Experimental procedure

**ALD AlN**

The aluminium nitride films in this study were deposited using trimethyl aluminium (TMA) and a mixture of $N_2$ and $H_2$ plasma. The films were initially grown on 15X15mm silicon substrates to identify the ALD window. The Si substrates were prepared using a standard ultrasonic clean in acetone for 5 minutes, rinsed in isopropyl (IPA) and then in RO water prior to ALD. To identify the ALD windows, 200 cycles of AlN were grown on silicon and the thicknesses and refractive indices of the films were measured using a spectroscopic ellipsometer (Woollam M-2000) at wavelenghth, $\lambda$ = 633 nm. The measured data were fitted with the Cauchy model with a refractive index of 1.9 for AlN.

Once the ALD windows were identified, the optimised film was analysed both physically and electrically on GaN substrates.

**Physical analysis**

The AlN film was deposited on the layer structure illustrated in Figure 7.2.1a(i) and was characterised physically using X-ray photoelectron spectroscopy (XPS). This was used to confirm the presence of AlN and to calculate the band offsets between AlN and GaN. The GaN samples used in the XPS measurements were also cleaned using the standard, acetone, IPA and RO water clean prior to AlN deposition.

**Electrical analysis**

Electrical analysis was carried out on GaN MOS capacitors with two different layer structures illustrated in Figure 7.2.1a(i) and a(ii) and for simplicity throughout this chapter they will be referred to as layer structure 1 and 2 as labelled in the figure. Layer structure 1 consist of bare GaN on Si substrates while layer structure 2 contains a 5nm $SiN_x$ layer that was grown in-situ as part of the MOCVD wafer growth. In order to carry out the in-situ $SiN_x$

etch and ALD deposition described in chapter 6 with AlN films as an interlayer the following steps were taken:

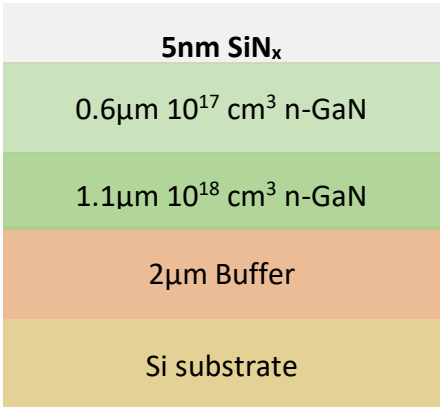
1. AlN ALD windows were identified using Si samples
2. AlN films with two different thicknesses, 2nm and 4nm were deposited on layer structure 1 after an $N_2$ 150w 5 minute plasma pretreatment. A 20nm $Al_2O_3$ film was then deposited on the AlN film. The final structure is shown in figure 7.2.1 b(ii).
3. Films were characterised electrically and compared to samples that also had the $N_2$ pretreatment but only had a 20nm $Al_2O_3$ grown on layer structure 1.
4. The thickness that produced the most favourable electrical characteristics was then used for the in-situ etching and ALD process. Here, the $SiN_x$ was etched using $SF_6$ plasma and transferred under vacuum to the ALD chamber, where the $N_2$ plasma pretreatment was performed, an AlN film was deposited which was followed by a 20nm thermal $Al_2O_3$ film.

All the GaN-based samples used for electrical characterisation were cleaned using the standard acetone, IPA and RO water clean prior to plasma processing.

**Layer structure 1**


a(i)

**Layer structure 2**




a(ii)

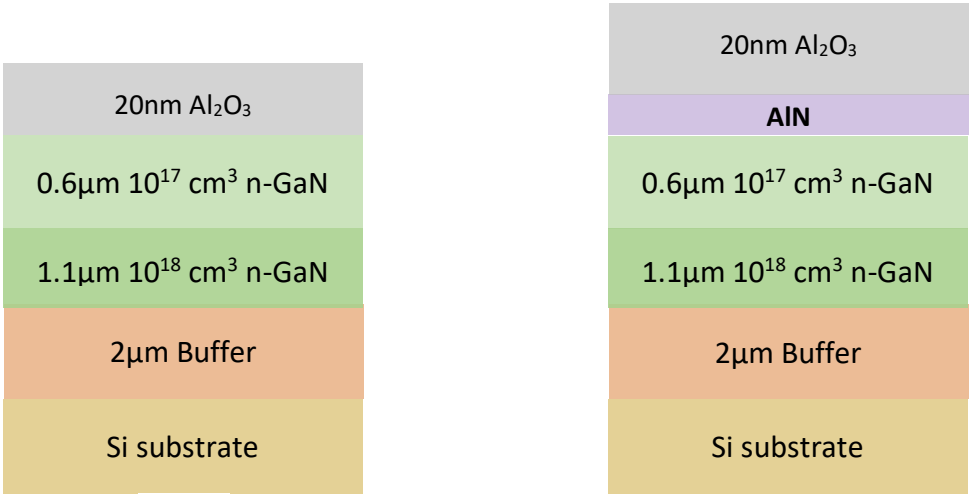



**Figure 7.2.1: Layer structure of GaN MOS capacitor used a(i)without SiNx a(ii) an b(i) with 20nm $Al_2O_3$ and b(ii) AlN/$Al_2O_3$ gate stack**

The following section describes in detail the parameters that were varied in order to identify the ALD windows and to obtain the optimised AlN films.

## 7.3 ALD windows

In order to optimise the AlN growth conditions, several process parameters have been investigated. These include $N_2$:$H_2$ gas flow ratio, substrate temperature, TMA and plasma exposure and purge time, RF power and chamber pressure. Table 7.3.1 outlines the base values used and the range of each parameter examined. Therefore, unless otherwise stated the base value for each parameter remains fixed.

| Parameters | Base value | Range |
|---|---|---|
| Plasma gas ratio | - | 1:6 – 6:1 $N_2$:$H_2$ |
| Temperature | 250$^0$C | 150 - 400$^0$C |
| TMA exposure time | 20ms | 10 - 80ms |
| TMA purge time | 3s | 0.5 - 5s |
| Plasma exposure time | 15s | 5 - 40s |
| Plasma purge time | 3s | 0.2- 12s |
| Applied power | 200W | 5 – 400W |
| Applied pressure | 15mTorr | 5 – 80mTorr |

**Table 7.3.1: Base values and range of parameters used**

- **Gas flow ratio**

The effect of the gas flow ratio on growth rate and refractive index was investigated by varying the individual flow rates of the gases, but the total flow rate was kept constant at 20sccm. The plasma gas ratios ranging from one that is hydrogen rich (1:6 $N_2$:$H_2$) to one that is nitrogen rich (6:1 $N_2$:$H_2$) were used. The results are displayed in Figure 7.3.1. It can be seen that constant growth rates and refractive indices were achieved for plasmas that were either hydrogen or nitrogen rich. Hydrogen rich plasmas show improvement in film properties where refractive indices of 1.9 and above were achieved while nitrogen rich plasmas only produced films with indices that were 1.8 and below. Growth rate also increased from $0.0612 \pm 0.0014$nm/cycle for samples that had a higher hydrogen flow rate to $0.072 \pm 0.0066$nm/cycle for samples that had a higher nitrogen flow rate. The increased growth rate of the plasmas with lower hydrogen concentration could be a result of the low supply of hydrogen radicals and ions that lead to an inadequate reduction of the alkyl groups which has also caused a reduction in the refractive index [4].

The following depositions that were carried out therefore used a gas flow ratio of 1:2 $N_2$:$H_2$ (6.7:13.3 sccm).

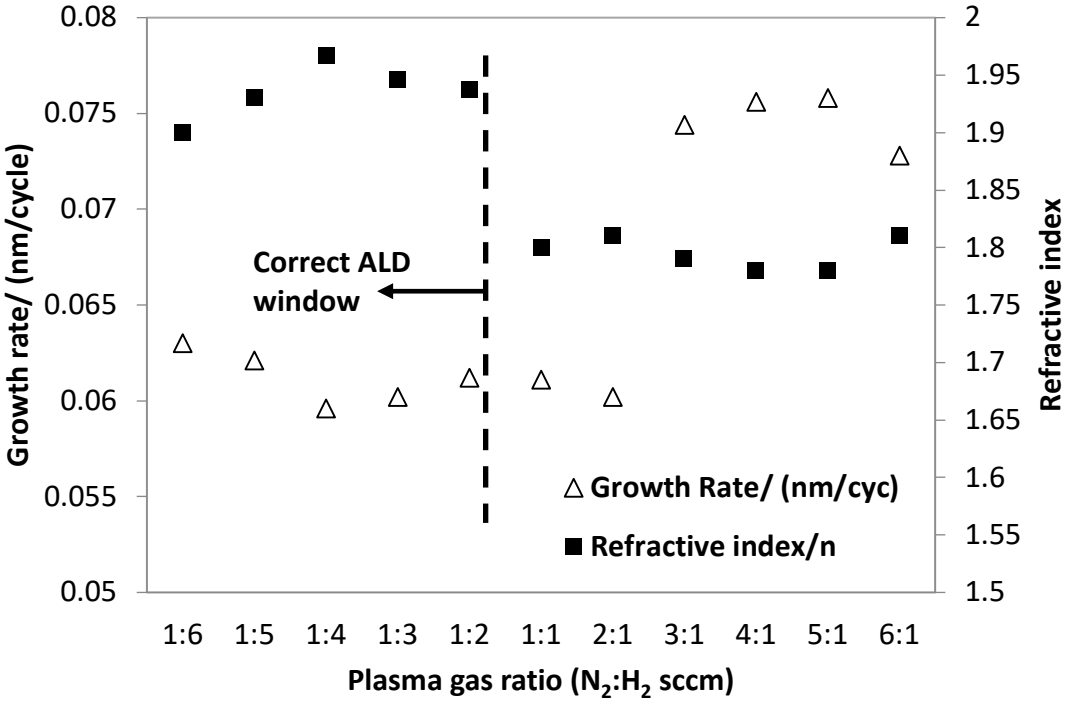



**Figure 7.3.1: Growth rate and refractive index of AlN as a function of plasma gas ratio**

- **Temperature window**

The effect of temperature on growth rate and refractive index of AlN films was examined for temperatures ranging from $150^0$C to $400^0$C with a gas flow ratio of 1:2 $N_2$:$H_2$. As shown in Figure 7.3.2, at temperatures above $200^0$C, a constant growth rate of 0.064 ± 0.0007nm/cycle and a refractive inactive index of 1.85 ± 0.0075 were achieved. A 59% decreased in growth rate was observed from 0.159 to 0.0656 nm/cycle when the temperature was changed from 150 to 250°C. Further, at temperatures below $250^0$C, poor film qualities with refractive indices of 1.59 and below achieved. The higher growth rate and low refractive indices are a result of the condensation of TMA at low temperatures leading to CVD type reactions.

From this ALD window it was decided that the film deposition in the following section were therefore carried out at $300^0$C.

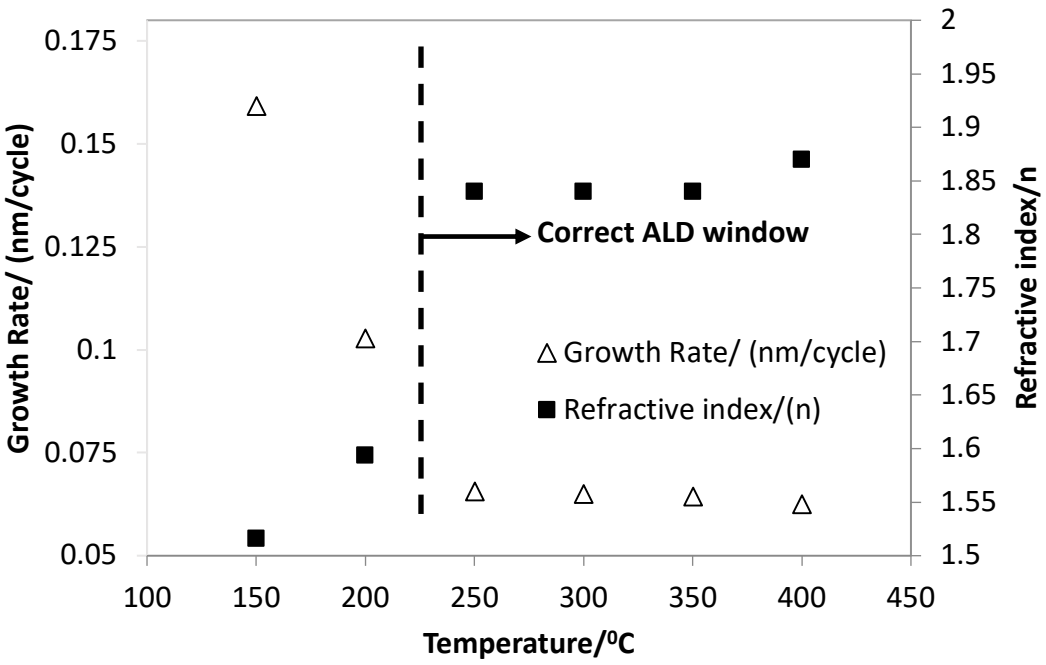



**Figure 7.3.2: Growth rate and refractive index of AlN as a function of temperature**

- **TMA exposure time**

The effect of TMA exposure times on the growth rate and refractive index of deposited films were explored by varying the exposure time from 10ms to 80ms with a gas flow ratio of 1:2 $N_2$:$H_2$ at $300^0$C. As can be seen in Figure 7.3.3, a constant growth rate of 0.067 ± 0.0027nm/cycle and a refractive index of 1.87 ± 0.0051 were achieved for precursor

exposure times of 20ms and above. An increase in the refractive index from 1.7 to 1.9 can be seen when the precursor exposure time was increased from 10 to 20ms.

The lower growth rate is most likely a result of insufficient coverage of TMA molecules on the sample surface leading to poor film quality. The TMA exposure times for the following processes was hence chosen to be 20ms.

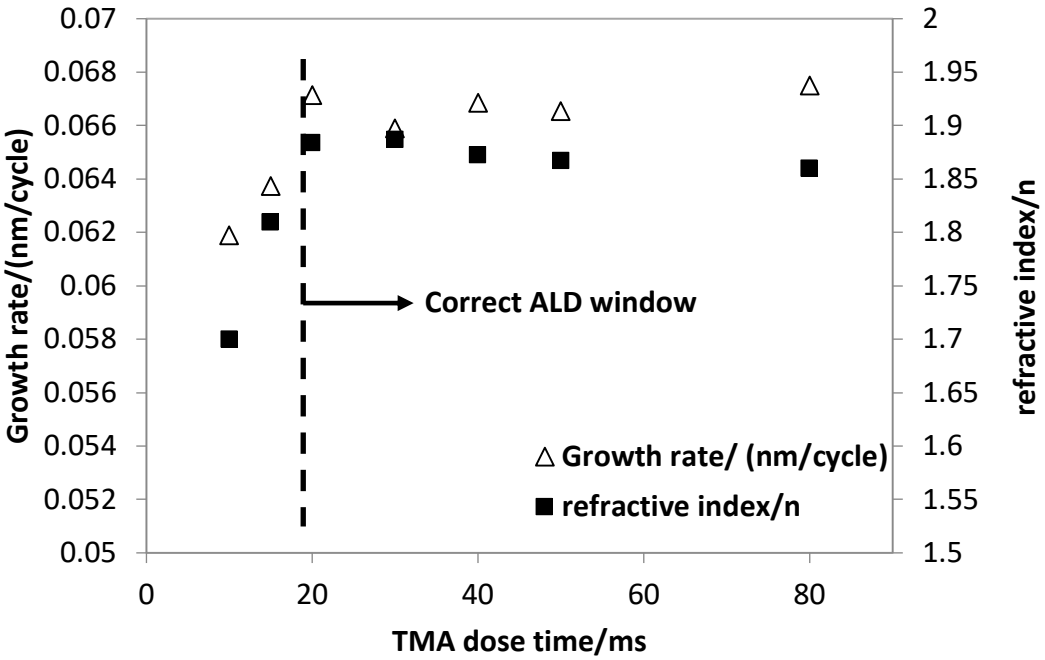



**Figure 7.3.3: Growth rate and refractive index of AlN as a function of TMA exposure time**

- **TMA purge time**

To examine the effect of TMA purge times on the quality of deposited films, the time was varied from 0.5s to 5s with a TMA exposure time of 20ms, a gas flow ratio of 1:2 $N_2$:$H_2$ at $300^0$C. As can be seen in Figure 7.3.4 a slight decrease in growth rate was obtained from 0.069 to 0.067 nm/cycle when the purge time increased from 0.5s to 3s. However, no significant change in the refractive index was observed. Only a slight increase in the refractive index from 1.86 to 1.87 was observed when the purge time was increased. TMA purge times below 0.5 s couldn't be examined because 0.5s was the machine's limit for the precursor purge time. The slight increase in growth rates at purge times lower than 3s might be a result of insufficient removal of byproducts from the chamber.

The TMA purge time was chosen to be 3 seconds.

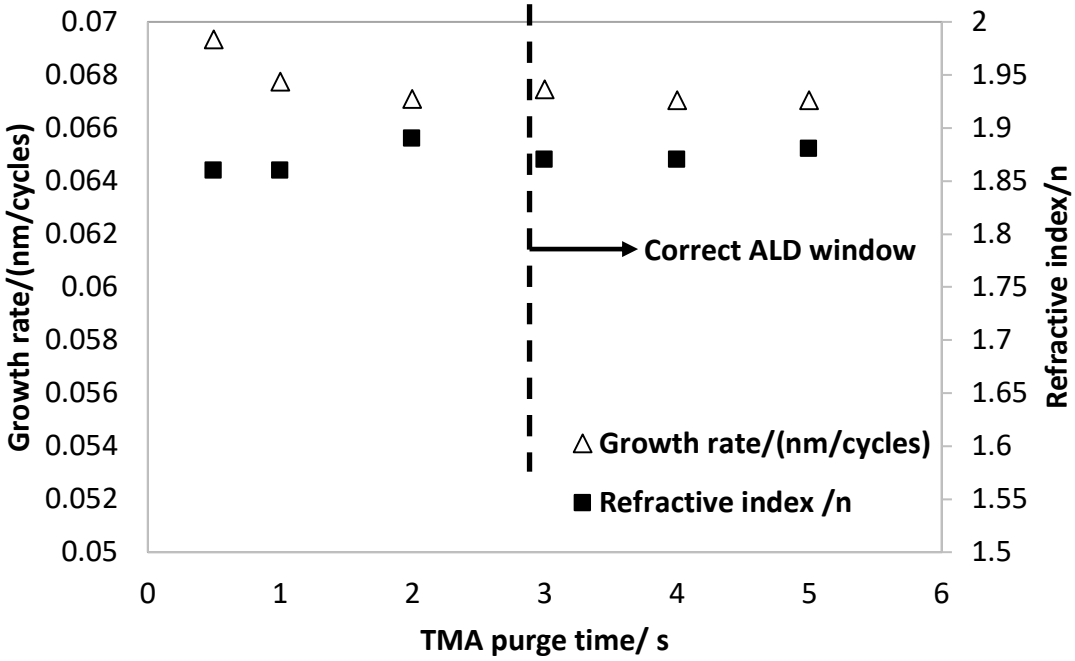



**Figure 7.3.4: Growth rate and refractive index of AlN as a function of TMA purge time**

- **Plasma exposure time**

The effect of plasma exposure time has been evaluated for times ranging from 5 to 40 seconds with a TMA exposure time of 20ms, TMA and plasma purge time of 3s, plasma gas ratio of 1:2 $N_2$:$H_2$ at $300^0$C. The results shown in Figure 7.3.5 indicate a constant growth of 0.064 $\pm$ 0.0002 and a refractive index of 1.88 $\pm$ 0.0037 for times above 15s. An enhancement in the film properties is observed in the increase in refractive index from 1.72 to 1.88 $\pm$ 0.0044 when the exposure time increased from 5 to 15s. It can also be noticed that the growth rate at 5s is slightly higher (6%) compared to exposure times equal to and above 15ms. The higher growth rate and low refractive index for the films below 5s might be due to higher impurity content of the under exposed films. The higher thickness may also be due to oxide formation due to the instability of under exposed films [1].

The plasma exposure time was therefore set again at 20s for subsequent depositions.

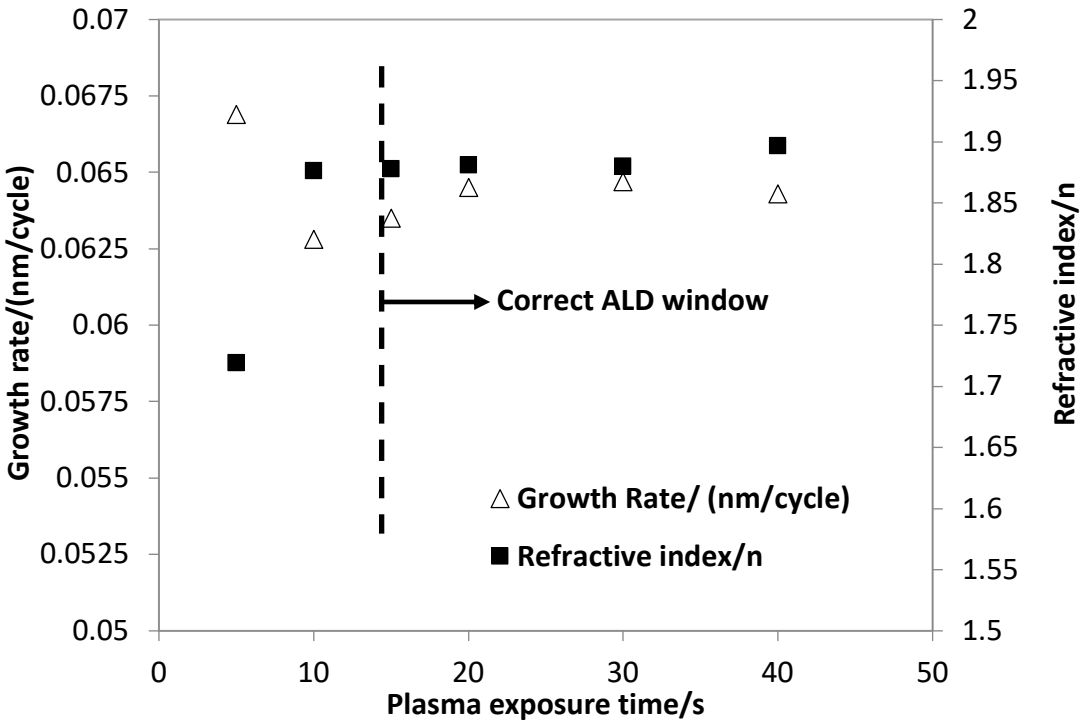



**Figure 1.3.5: Growth rate and refractive index of AlN as a function of plasma exposure time**

- **Plasma gas purge times**

The effect of plasma purge times on film properties and growth rate has been examined by varying the purge time from 200ms to 12 second. It can be seen from Figure 7.3.6 that a constant growth rate of 0.065 ± 0.004 nm/cycle and a refractive index of 1.89 ± 0.003 have been achieved for purge times above 2 seconds. The slight decrease (4.5%) in growth rate and the increase in the refractive index 1.79 to 1.88 when plasma gas purge time was increased from 200ms to 2s may be a result of byproducts not being completely removed from the chamber for purge times below 2s.

The plasma purge time for the next ALD processes was fixed at 3s.

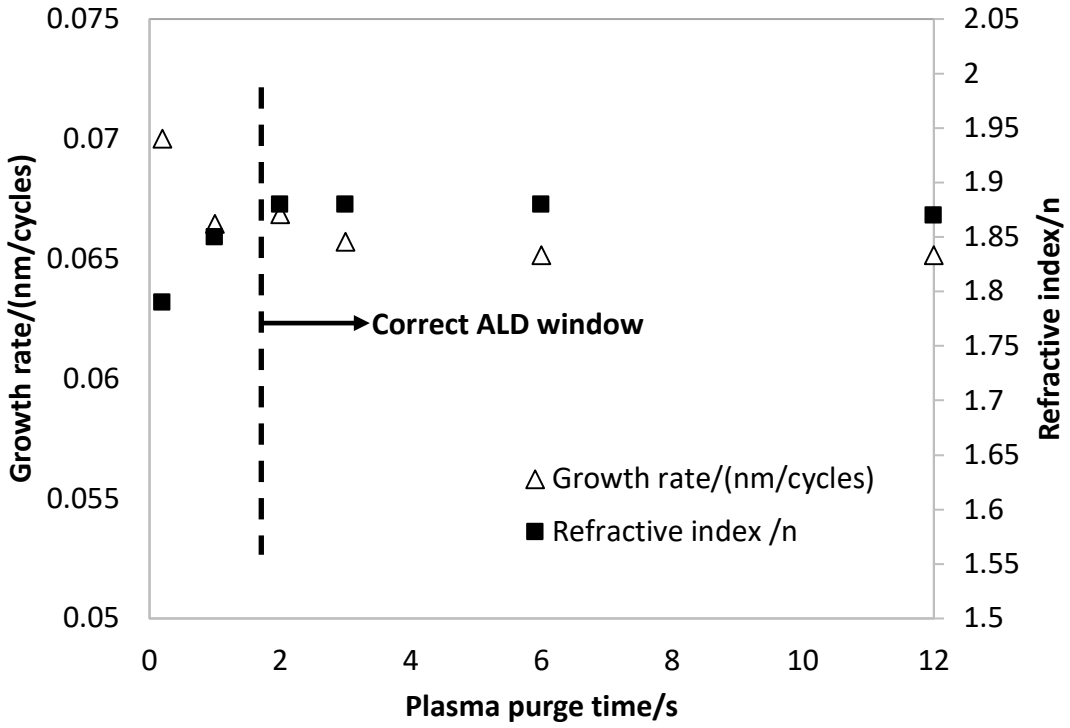



**Figure 7.3.6: Growth rate and refractive index of AlN as a function of plasma purge time**

- **Applied Power**

The effect on growth rate and refractive index as a function or varying power from 5W to 400W are displayed in Figure 7.3.7. A constant growth rate of 0.063 $\pm$ 0.005 nm/cycle and refractive index of 1.85 $\pm$ 0.02 have been achieved for powers above 150W. The low growth rate at lower applied power is however contradictory to that reported in literature [1]. The reduction in growth rates at lower powers may be due to the low activation energy provided from plasma to the reactions. An increase in growth rate at low powers, as reported in [1], may not have been observed in this case because deposition was carried out at sufficient purge time hence all the byproducts are removed. The increase in refractive index from 1.65 to 1.88 is an indication of better film properties at higher powers.

The plasma power was therefore chosen to be 200W for the subsequent processes.

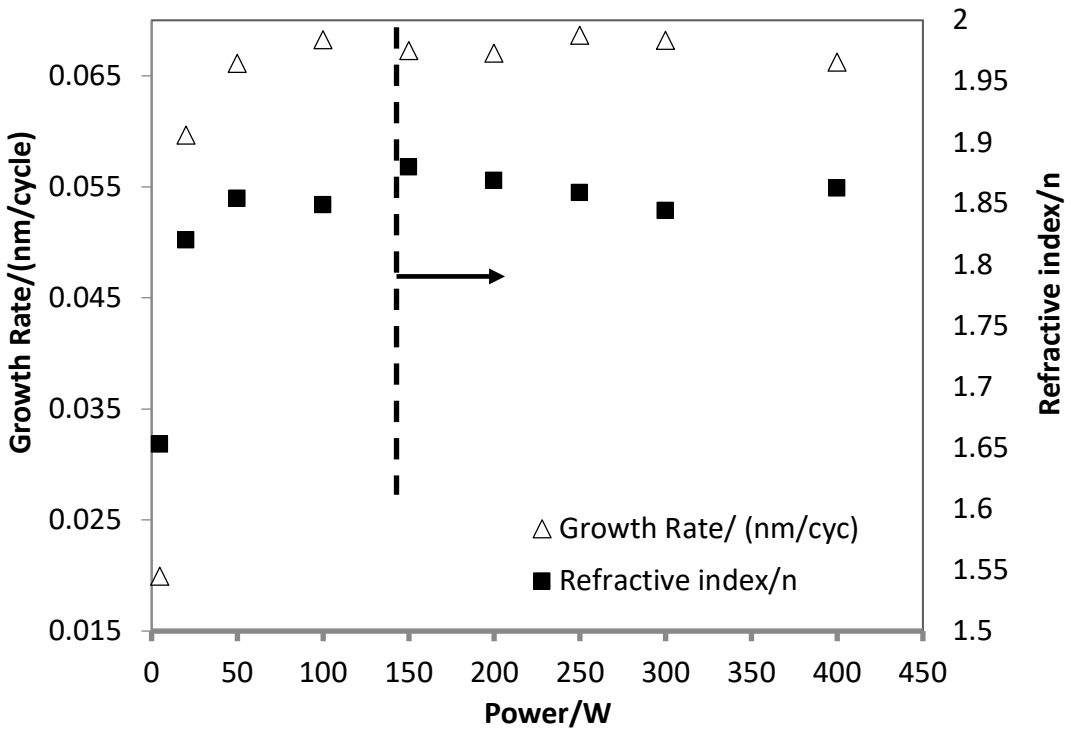



**Figure 7.3.7: Growth rate and refractive index of AlN as a function of plasma**

- **Applied Pressure**

Figure 7.3.8 represents the effect of pressure on both the growth rate and refractive index. The chamber pressure has been varied from 5 to 80mTorr. As the pressure increases the growth rate falls from 0.073nm/cycle at 5mTorr to 0.055nm/cycle at 80mTorr. The refractive index on the other hand decreased from 1.91 to 1.82. It can be observed that both the growth rate and refractive index have decreased as the pressure has increased and no constant growth regime has been identified. It has been shown in previous studies that an increase in the pressure has resulted in a decrease in the electron density [5]. Electrons, though collisions in the plasma, help in the creation of plasma radicals, ions and photons [6]. These species then bring about reactions when they arrive at the surface of the substrate. To understand the effect of plasma further, the following section looks in detail at the plasma residence time.

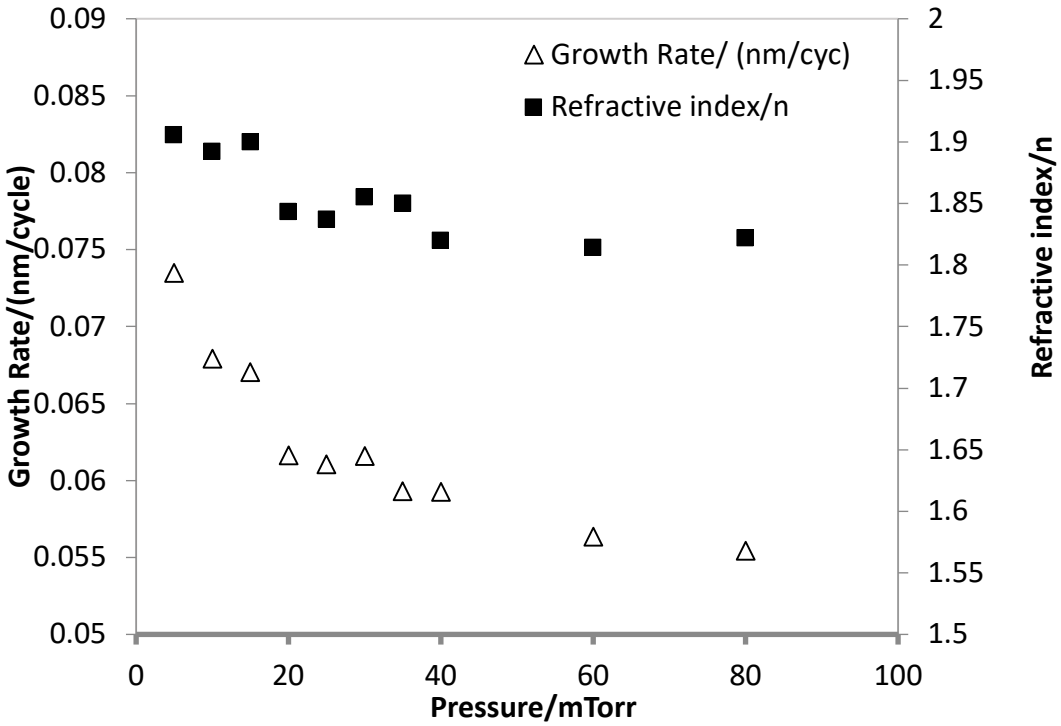



**Figure 7.3.8: Growth rate and refractive index of AlN as a function of plasma pressure**

- **Plasma residence time**

The effect of the plasma on the AlN film properties has been further explored by investigating the influence of plasma residence time, $\tau$. During the plasma step, the plasma consists of the co-reactants and the reaction byproducts. These by-products can be incorporated back into the films increasing the impurity levels. $\tau$ is the duration for which these by-products remain in the chamber before being pumped out [7]. It is a function of the volume of the reactor, V and the total gas flow rates, q as given by $\tau$=V/q (equation 7.1)**.** The larger the flow rates, the faster the by-products are pumped out. The flow rate can be expressed using the ideal gas laws, in terms of standard pressure, $p_0$ (760mTorr) and the measured chamber pressure, P [7]. The total gas flow ratio was kept constant at 1:2 $N_2$:$H_2$ and the actual pressure was measured while varying the total flow rate from 10 to 100sccm. The volume of the reactor was 13.8L[7]. Table 7.3.2 summarises the effect on refractive index for various calculated plasma residence times. Figure 7.39 is a graphical representation of the effects of plasma residence time, pressure and flow rates. An increase in the total gas flow rate from 10 to 20sccm enhances the refractive index from 1.72 to 1.9, this can also be corelated to the decrease in plasma resident time from 1.63 to 0.81s. However further increase in gas flows do not changed the refractive index markedly;

this could be due to the increase in pressure that arises due to the increase in gas flows. As discussed earlier higher pressures can lead to a reduction in the electron density in the plasma.

Therefore, low pressure and high gas flows are favourable with regards to film properties and help produce films with refractive indices closer to the theoretical value of ideal AlN.

$$\tau = \frac{V}{q} \qquad 7.1$$

where $q = \frac{q_0 p_0}{P}$

$$\tau = \frac{PV}{q_0 p_0} \qquad 7.2$$

V = Effective volume of the reaction chamber, q = volumetric flow rate,

$P = \text{standard pressure } (760\text{mTorr})$, $p_0 = \text{chamber pressure}$,

$q_0 = \text{flow rate of the plasma gasses}$

| Pressure/ mTorr | Gas flow/ ($N_2$:$H_2$ sccm) | Total flow rate/ sccm | Plasma residence time, $\tau$ / sec | Refractive index/ n |
|---|---|---|---|---|
| 15 | 3.3:6.7 | 10 | 1.63 | 1.724 |
| 15 | 6.7:13.3 | 20 | 0.81 | 1.9 |
| 29.9 | 26.7:53.3 | 80 | 0.41 | 1.89 |
| 36.8 | 33.3:66.7 | 100 | 0.4 | 1.894 |

**Table 7.3.2: Effect of plasma resident time on refractive index**

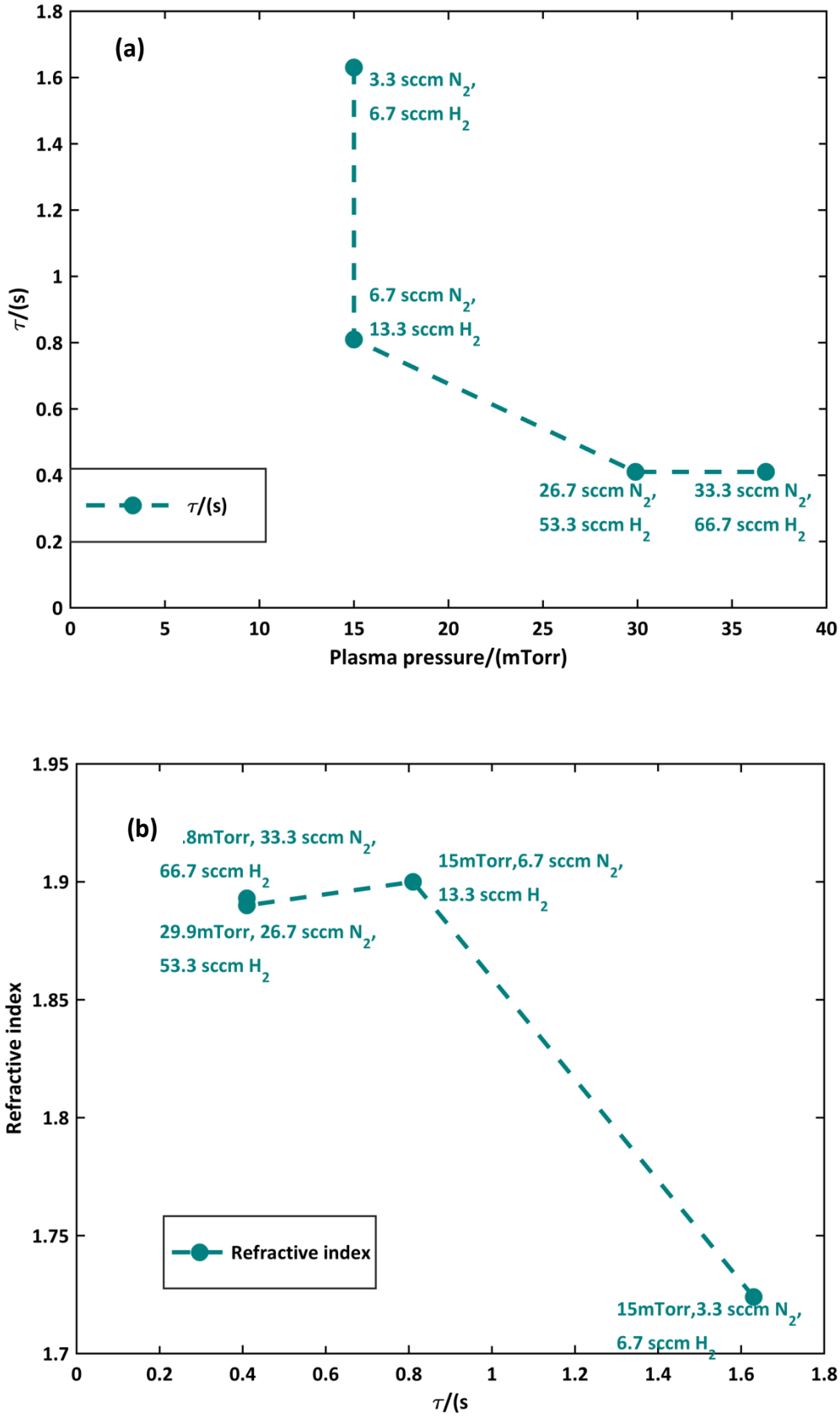



**Figure 7.39: (a) Effect of pressure and gas flow ratio on $\tau$ and (b) effect of $\tau$ on refractive index of AlN**

After examining all the factors discussed previously, the following values were then chosen for each parameter to provide a well optimised AlN layer:

TMA dose: 20ms

Plasma exposure: 20s

TMA and plasma purge: 3s

Temperature: $300^0$C

Plasma gas ratio: 6.7sccm: 13.3sccm

Plasma power: 200W

Pressure: 15mTorr

The subsequent sections provide the physical characterisation of an AlN film that was deposited using the optimised parameters. It also provides the electrical characterisation of the film when used as an interlayer between GaN and $Al_2O_3$.

# 7.4 Characterisation of AlN

The AlN films grown on GaN MOSCAP structures described in Figure 1.2.1a(i) have been analysed physically by using X-ray photoelectron spectroscopy (XPS) and electrically by measuring their C-V and I-V properties. Details of the analyses are described below. All XPS measurements were performed by collaborators at the University of Liverpool.

### 7.4.1 Physical analysis

Two different thicknesses, 5nm and 20nm of AlN were grown on GaN MOS capacitor wafer structures and analysed using XPS to confirm the presence of atomic layer deposited AlN. The sample with 20nm AlN was used to produce information regarding the bulk properties of AlN and is illustrated in Figure 7.4.1. The 5nm sample on the other hand, was used to provide data on the band offsets between AlN and GaN, which is depicted in Figure 7.4.2.

The spectra shown in Figure 7.4.1 indicates the presence of AlN and that the film is thick enough that no Ga peaks (from the GaN surface below AlN) were obtained. However, a strong oxygen peak is present leading to the conclusion that there is some oxide in the AlN films. The spectra also suggest that there is also some carbon present in the films. There is also a peak at ~685 eV which is indicative of fluorine presence, this could be from the boxes in which the samples were kept.

The band gap data used when calculating the band offset shown in Figure 7.4.2 (as described in chapter 5) were taken from literature [8]. It shows that the conduction band offset (CBO) between AlN and GaN is 2.04eV, which is 2.9% lower than the reported value of 2.1eV [9]. The valence band offset (VBO) on the other was 0.61eV, which also is lower by 12.9% than the reported value of 0.7eV [9].

It is evident from the XPS data that the band offsets are not as high as those reported in the literature. This may be a consequence of the presence of oxygen and carbon in the AlN films and also due to the impurities present on the GaN surface. Although it confirms the presence of AlN on GaN, the XPS data also confirm that there is yet room for improvement of the AlN films.

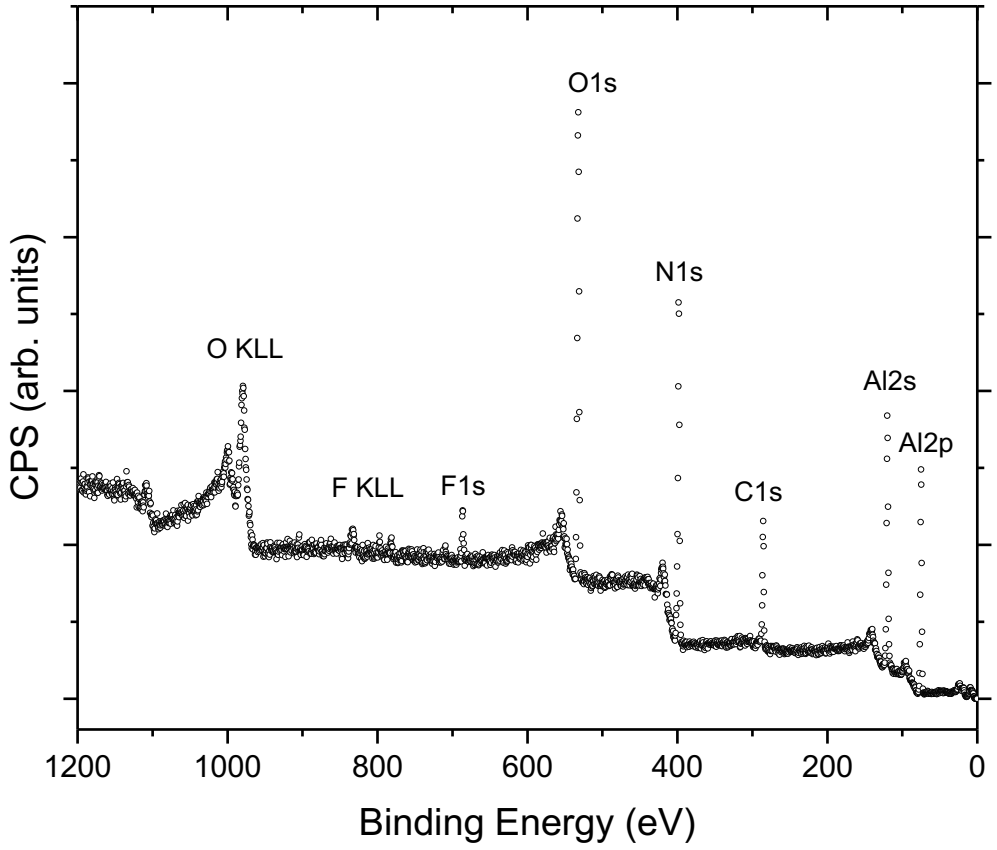



**Figure 7.4.1: Survey spectra for 20nm AlN**

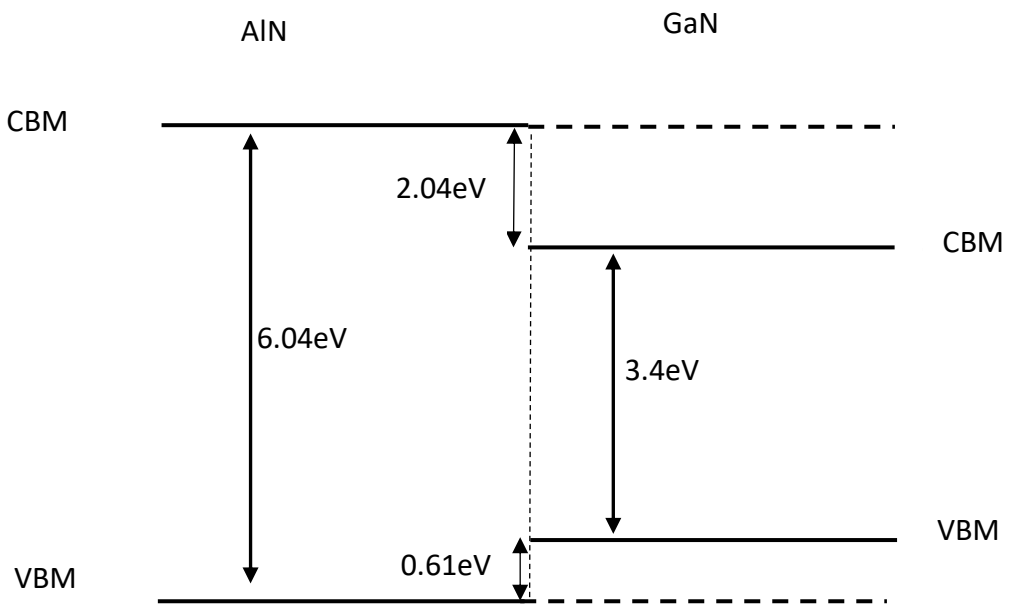



**Figure 7.4.2: Band alignment between interface of AlN and GaN (CBM= conduction band minimum and VBM= valence band minimum)**

### 7.4.2 Electrical analysis

The effect of AlN as an interlayer between GaN and $Al_2O_3$ was investigated electrically by performing capacitance-voltage and current-voltage measurements at room temperature. The GaN MOS capacitor samples were first exposed to an $N_2$ 150W 5min plasma pre-treatment followed by in-situ ALD of AlN. A 20nm $Al_2O_3$ was then deposited in-situ using thermal ALD at $200^0$C using TMA and $H_2O$ as precursors. Firstly, the thickness of the AlN was verified by testing samples with two different thicknesses; 2 and 4nm respectively. These results were then compared with MOSCAPs that had only an $N_2$ 150W 5min plasma pre-treatment followed by a 20nm thermal ALD $Al_2O_3$ layer. The film thickness that generated the best electrical data was then deposited on MOS capacitor that had an in-situ SiN layer. The SiN layer was etched using an $SF_6$ plasma, transferred under vacuum to the ALD chamber where a $N_2$ 150W 5min plasma pre-treatment was performed and AlN and $Al_2O_3$ were deposited. The samples have not been treated with a forming gas anneal. A summary of the layer structures used and sample names are depicted in table 1.4.2. The layer structure of the capacitors with the films have been iterated again in figure 7.4.3.

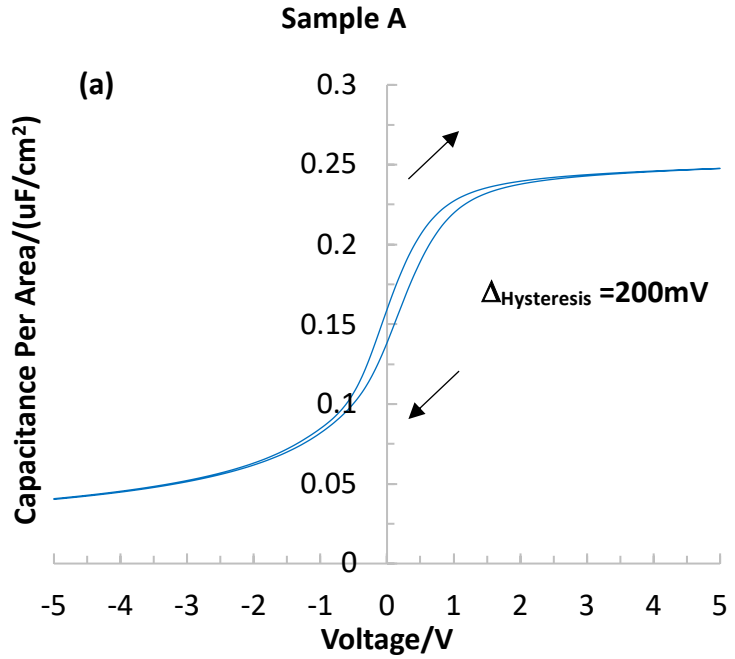
| Sample name | Layer structure | Gate stack |
|---|---|---|
| A | 1 | 20nm $Al_2O_3$ only |
| B | 1 | 4nm AlN/10nm $Al_2O_3$ |
| C | 1 | 2nm AlN/10nm $Al_2O_3$ |
| D | 2 | 2nm AlN/10nm $Al_2O_3$ |

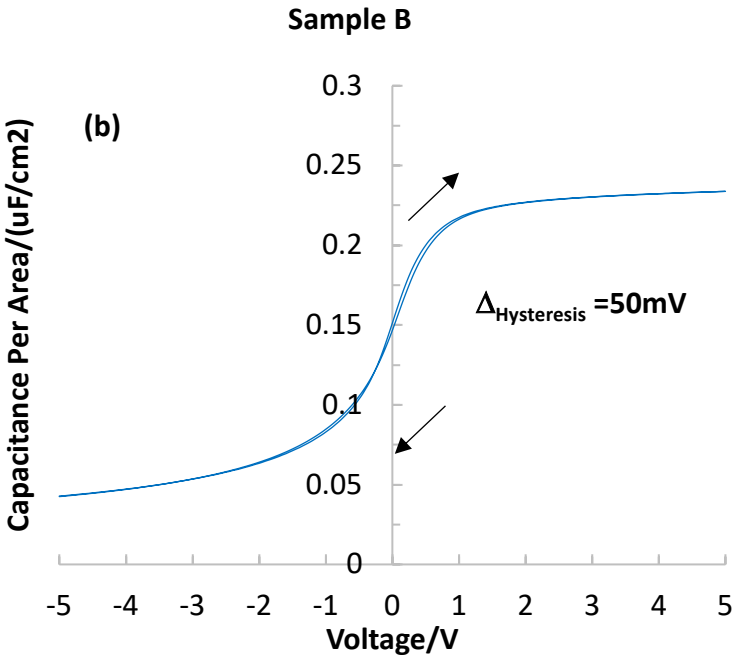
**Table 7.4.2: Summary of samples names, layer structure and gate stack used**


**Figure 7.4.3: Layer structure of GaN MOS capacitor with (i) 20nm $Al_2O_3$ and (ii) AlN/20nm $Al_2O_3$ gate stack**

**C-V hysteresis**

The C-V hysteresis, $\Delta_{Hysteresis}$ was measured at 1MHz and the data obtained for samples A, B and C are shown in Figure 7.4.4. Sample A produced a hysteresis of 200mV while a 50mV hysteresis was achieved for the samples that incorporated an AlN layer. Therefore, the insertion of an AlN layer has reduced the C-V hysteresis by 75%.


Sample A
(a)
Capacitance Per Area/(uF/cm²)
0.3
0.25
0.2
0.15
0.1
0.05
0
-5 -4 -3 -2 -1 0 1 2 3 4 5
Voltage/V
ΔHysteresis =200mV


Sample B
(b)
Capacitance Per Area/(uF/cm2)
0.3
0.25
0.2
0.15
0.1
0.05
0
-5 -4 -3 -2 -1 0 1 2 3 4 5
Voltage/V
ΔHysteresis =50mV

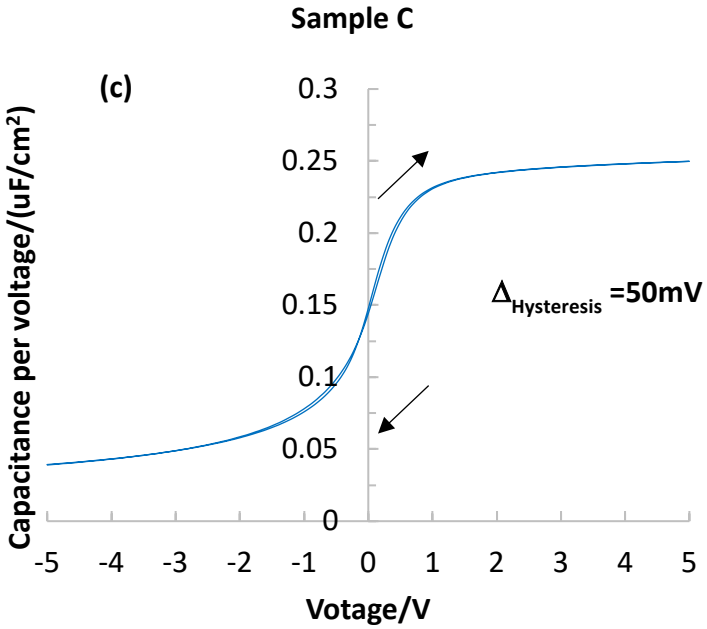
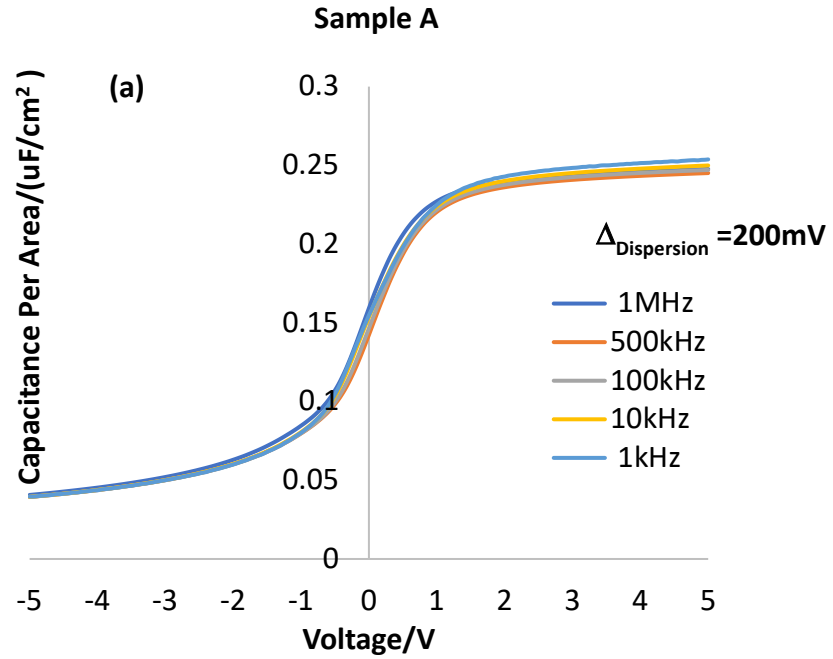
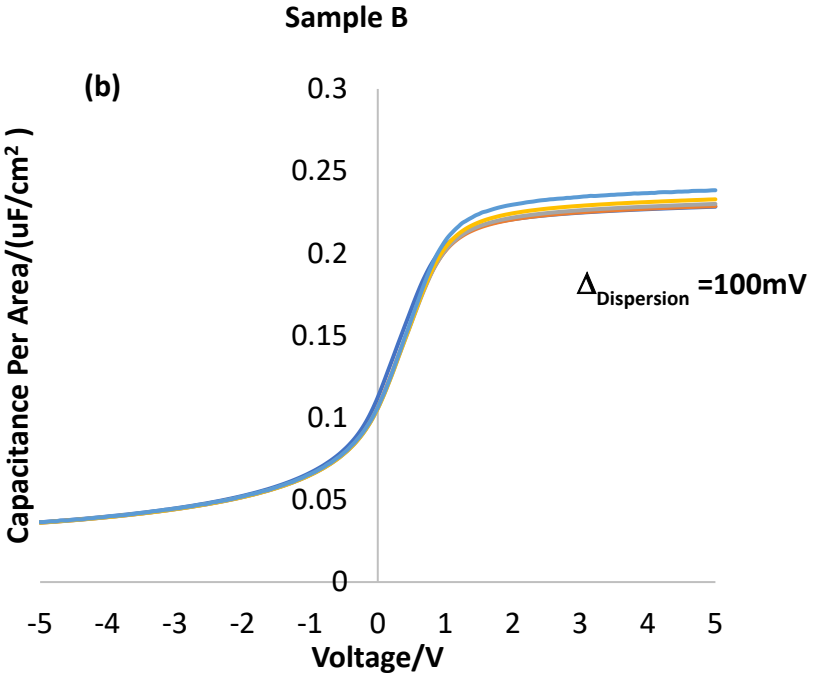



**Figure 7.4.4: C-V hysteresis of GaN MOSCAP with (a) 20nm $Al_2O_3$ gate dielectric, (b) 4nm AlN/20nm $Al_2O_3$ gate stack and (c) 2nm AlN/20nm $Al_2O_3$ gate stack**

**Frequency dispersion**

Frequency dispersion, $\Delta_{Dispersion}$, data was obtained by performing C-V measurements from 1MHz to 1kHz and is shown in Figure 7.4.5. The data indicates that the insertion of a 4nm AlN (sample B) has reduced the dispersion from 200mV to 100mV. This has further been reduced to 50mV in sample C, the sample with 2nm of AlN. This suggests a reduction in the interface traps with the 2nm AlN layer. It can also be noticed that a change in the accumulation capacitance is also observed in each sample when the frequency was changed from 1MHz to 1kHz. Sample A produced a difference of 0.006 µF/cm$^2$ in the accumulation capacitance while in sample B increased this to 0.010µF/cm$^2$ and this increased further to 0.012µF/cm$^2$ in sample C. The change in the accumulation capacitance as a function of frequency suggests the presence of border traps in the dielectric.


Sample A
(a)
Capacitance Per Area/(uF/cm² )
0.3
0.25
0.2
0.15
0.1
0.05
0
-5 -4 -3 -2 -1 0 1 2 3 4 5
Voltage/V
Δ Dispersion =200mV
1MHz
500kHz
100kHz
10kHz
1kHz


Sample B
(b)
Capacitance Per Area/(uF/cm² )
0.3
0.25
0.2
0.15
0.1
0.05
0
-5 -4 -3 -2 -1 0 1 2 3 4 5
Voltage/V
Δ Dispersion =100mV

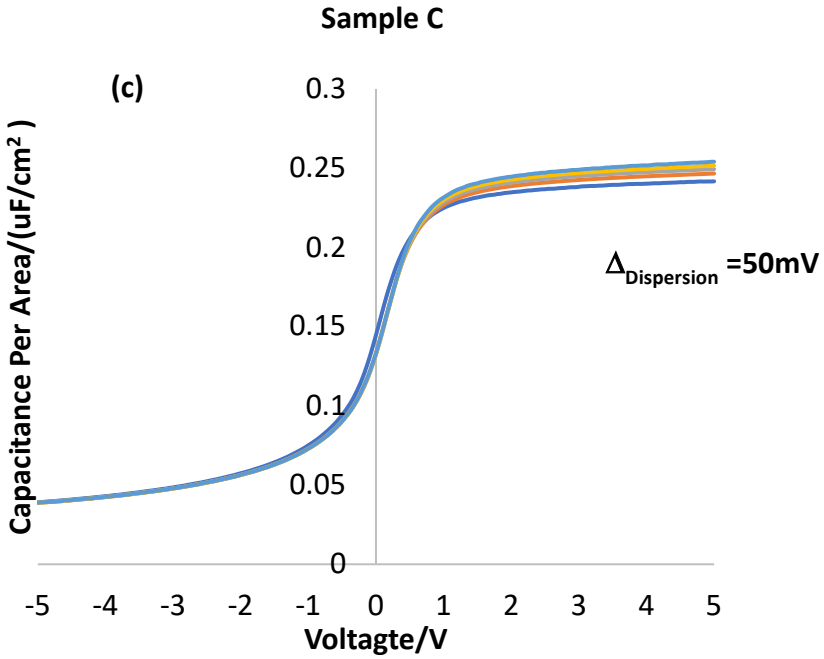



**Figure 7.4.5: Frequency dispersion of GaN MOSCAP with (a)20nm $Al_2O_3$ gate dielectric, (b) 4nm AlN/20nm $Al_2O_3$ gate stack and (c) 2nm AlN/20nm $Al_2O_3$ gate stack**

### Accumulation capacitance

Figure 1.4.6 depicts the C-V curve at 1MHz of the samples with the two different AlN thicknesses. It can be seen that as the AlN thickness increases the accumulation capacitance decreases. This is due to the total series capacitance arising from the two films.

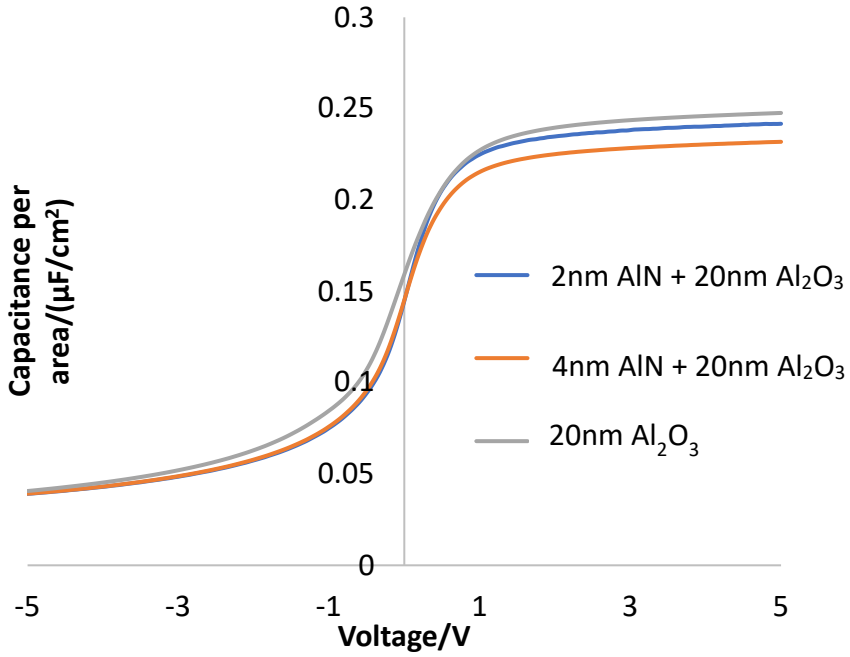



**Figure 7.4.6: Effect on accumulated capacitance of 2nm and 4nm AlN**

**Stress voltage measurements**

Figure 7.4.7 depicts the C-V hysteresis obtained during stress voltage measurements. These were measured at 10kHz, while varying the range of voltage from -5 to 0V and back to -5V then -5 to 1V and back to -5V and so on. The x-axis values denote the final voltage value to which the voltage was swept. The increase in C-V hysteresis with the voltage range is more prominent in the samples that only had a 20nm $Al_2O_3$ layer. It increased the least for the samples that had the 2nm AlN interlayer. This proves further that the AlN interlayer has caused a reduction in the interface traps.

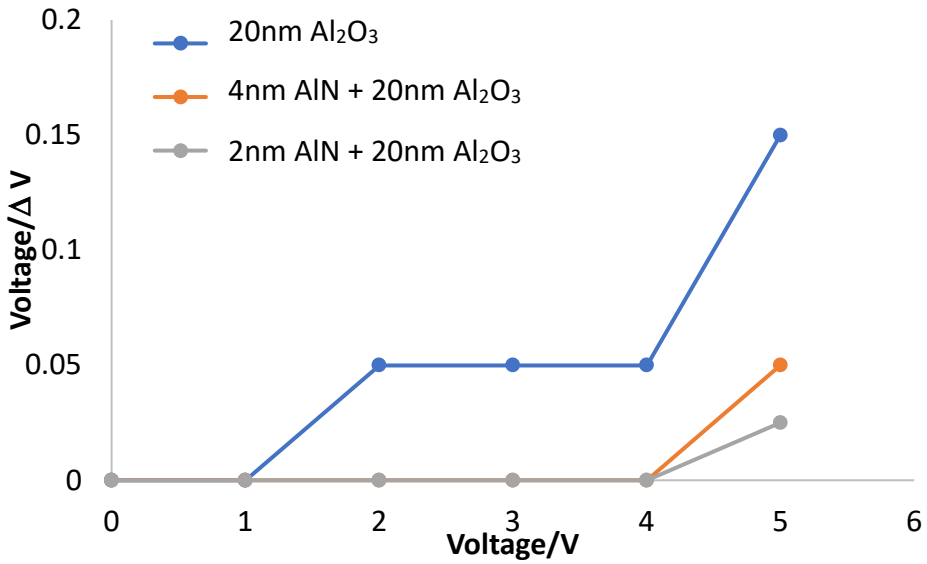



**Figure 7.4.7: Effect on hysteresis during stress voltage measurement**

**C-V slope**

Figure 7.4.8 display the differentiation of the C-V cures obtained at 1MHz. The samples C, with the 2nm AlN layer, generated the highest slope with 0.16µF/cm$^2$V, while the sample A, with no AlN interlayer showed a slope of 0.12µF/cm$^2$V. The increase in the slope with the 2nm AlN interlayer is a consequence of the reduction in the interface traps between the $Al_2O_3$ – GaN interface.

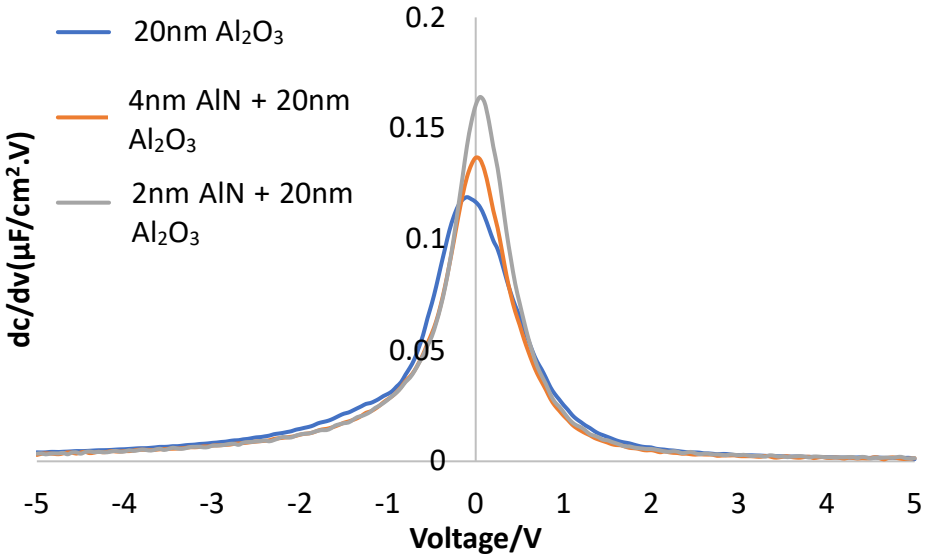
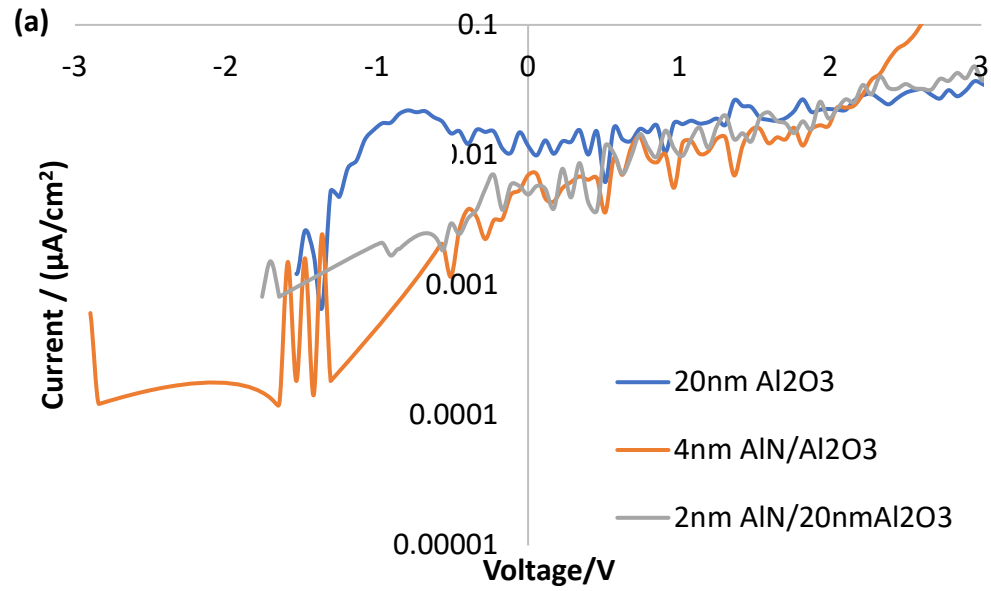



**Figure 7.4.8: Comparison of C-V slope between samples with only 20nm $Al_2O_3$ and the AlN interlayer**

**I-V sweep**

The leakage current and breakdown voltage of the films are shown in Figure 7.4.9. A leakage current of 0.016μA/cm$^2$ was obtained for the sample with only $Al_2O_3$ while those with the interlayer produced a leakage current of 0.0088μA/cm$^2$ for 4nm AlN and 0.0096 μA/cm$^2$ for 2nm AlN. However, the breakdown voltage shows that the samples with the AlN/$Al_2O_3$ gate stack had lower breakdown voltage than the single layer $Al_2O_3$ samples.



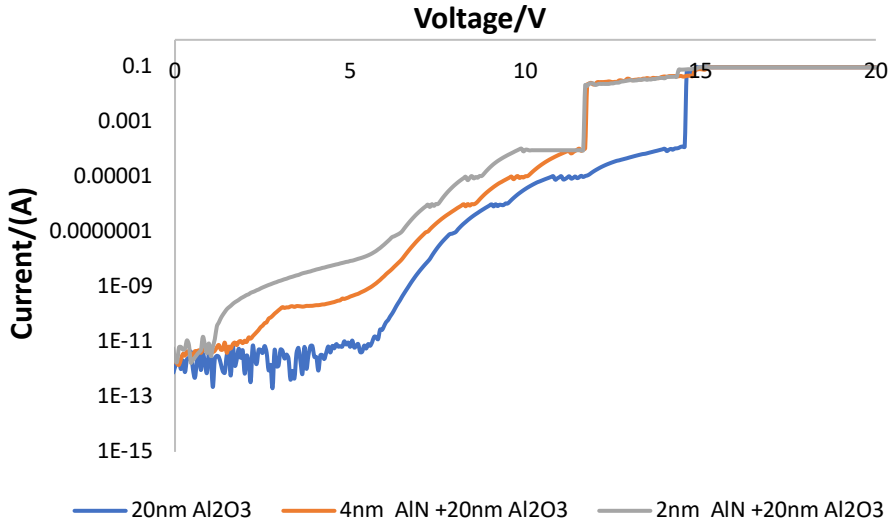



**Figure 7.4.9: (a) Comparative leakage currents of samples with only 20nm $Al_2O_3$ and the AlN/$Al_2O_3$ gate stacks (b)Comparative breakdown voltage data between samples with only 20nm $Al_2O_3$ and the AlN/$Al_2O_3$ gate stacks**

The results show that in comparison to the sample with no AlN (sample A) the presence of a 2nm AlN interlayer (sample C) reduced the $\Delta_{Dispersion}$ by 75% from 200mV to 50mV, reduced the $\Delta_{Dispersion}$ by 75% from200mV to 50mV and increased the C-V slope by 33%. The leakage current of the sample B (4nm AlN interlayer) was 45% lower than sample A. The leakage current in sample C was 10% higher than sample B, but still lower than with the $Al_2O_3$ only samples. However, the breakdown voltage of sample A was 14.6V while B and C were 11.6. The better electrical properties of the sample with the 2nm AlN interlayer may be a consequence of the change in the crystalline nature of AlN.

Taking in to consideration the lower hysteresis, frequency dispersion, leakage current, higher C-V slope and higher accumulated capacitance, a 2nm AlN layer was chosen to be deposited on layer structure 2 post SiN etch in the etching chamber. The results of which will be discussed in the next section.

**Electrical data of AlN on "in-situ" processed samples**

The in-situ SiN deposited in the final stage of the wafer growth of the sample shown in Figure 7.2.2(a)ii (layer structure 2) was first etched in the Cobra chamber of the cluster tool using the $SF_6$ process described in chapter 6 and transferred under vacuum to the ALD

chamber of the cluster tool where an $N_2$ 150W 5 minute plasma pre-treatment was performed prior to the 2nm AlN deposition using the optimised process described above. This was followed by thermal ALD deposition of a 20nm $Al_2O_3$ film (sample D). Figure 7.4.10 illustrates the C-V hysteresis and frequency dispersion measured for this sample. The hysteresis and frequency dispersion have increased to 500mV when the samples were processes in-situ.

Figure 7.4.11 portrays the graphs obtained when the C-V curves were differentiated. The C-V slope of sample D is higher than that of the sample A, but the highest slope achieved was still sample C. Figure 7.4.12 display the C-V hysteresis data obtained from stress voltage measurements for all the samples described above. In sample D, it can be seen that the hysteresis continues to increase after 2V when the bias range was increased, while in sample B and C a hysteresis only starts to appear after 4V. In comparison to sample B the hysteresis of sample C is 50% lower.

Figure 7.4.13 exhibit the leakage current and breakdown data for all the samples described above. The leakage current for the in-situ SiN samples was 0.023μA/cm$^2$, which is the highest of all the samples studied. The breakdown voltage too was lower than the other samples, at around 11.3V.

It can be concluded from the data presented in Figures 7.4.4 to 7.4.13 that the 2nm AlN interlayer enhanced the interface properties, however these properties haven't been translated to sample D that used layer structure 2, where the GaN surface was not exposed to the atmosphere. It may be that The $SF_6$ plasma that is used to remove the $SiN_x$ layer, fluorine terminates the GaN surface and the nucleation of the aluminium nitride on a fluorine terminated surface isn't identical to of a bare GaN surfaces of layer structure 1, resulting in different performance of deposited AlN films.

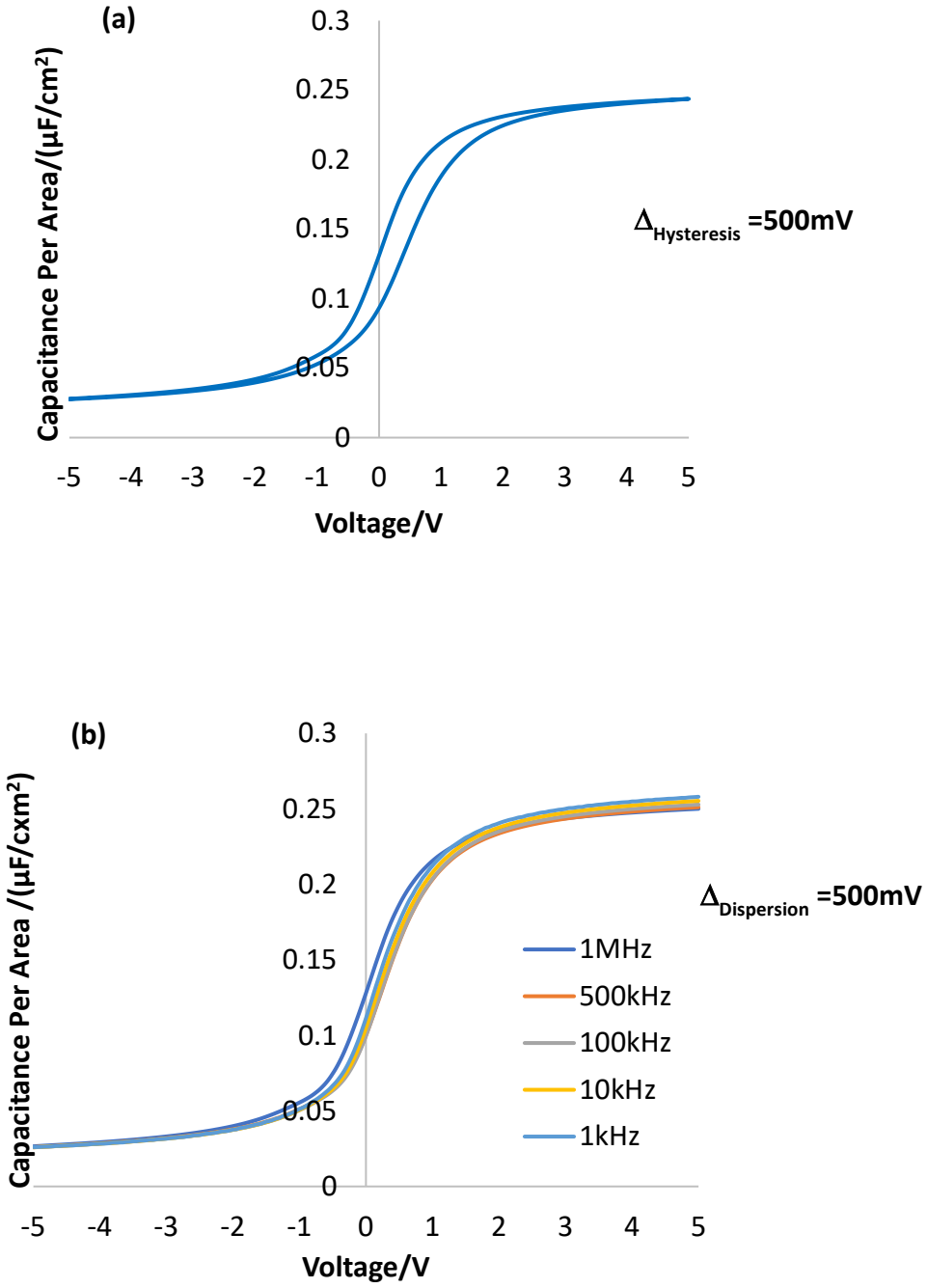



**Figure 7.4.10: Frequency dispersion of GaN MOSCAP with (a) C-V hysteresis and, (b) Frequency dispersion of in-situ SiNx etched + 2nm AlN/20nm $Al_2O_3$ gate stack**

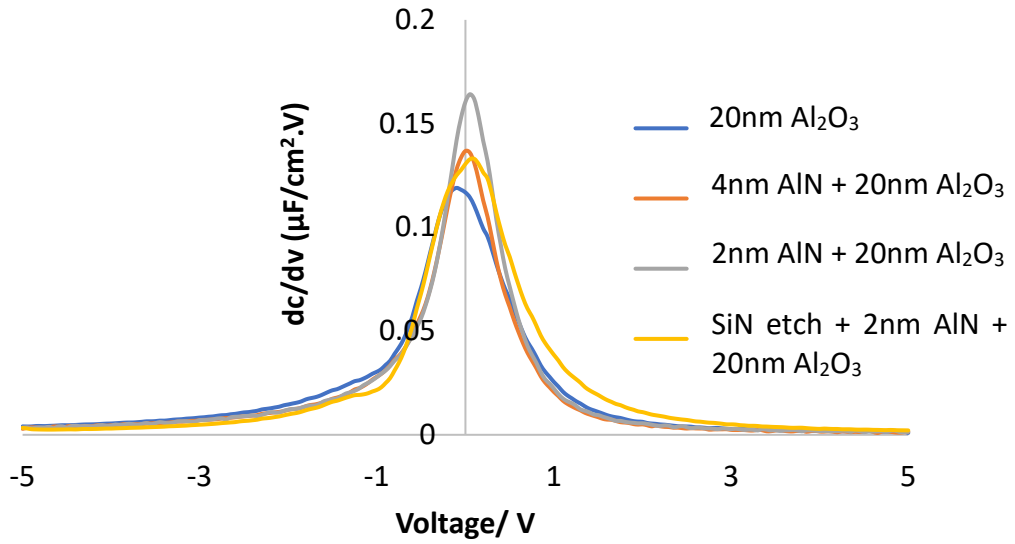



**Figure 7.4.11: Comparison of the slope of C-V curves for samples with only 20nm Al2O3, with AlN interlayer and the samples that went through in-situ etching**

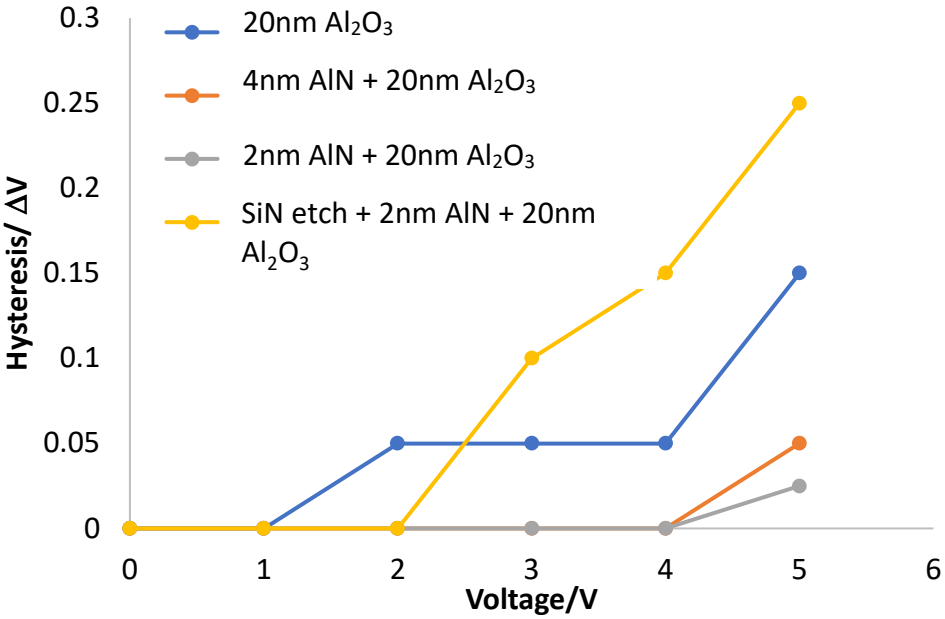



**Figure 7.4.12: Hysteresis obtained from stress voltage measurements for all the samples**

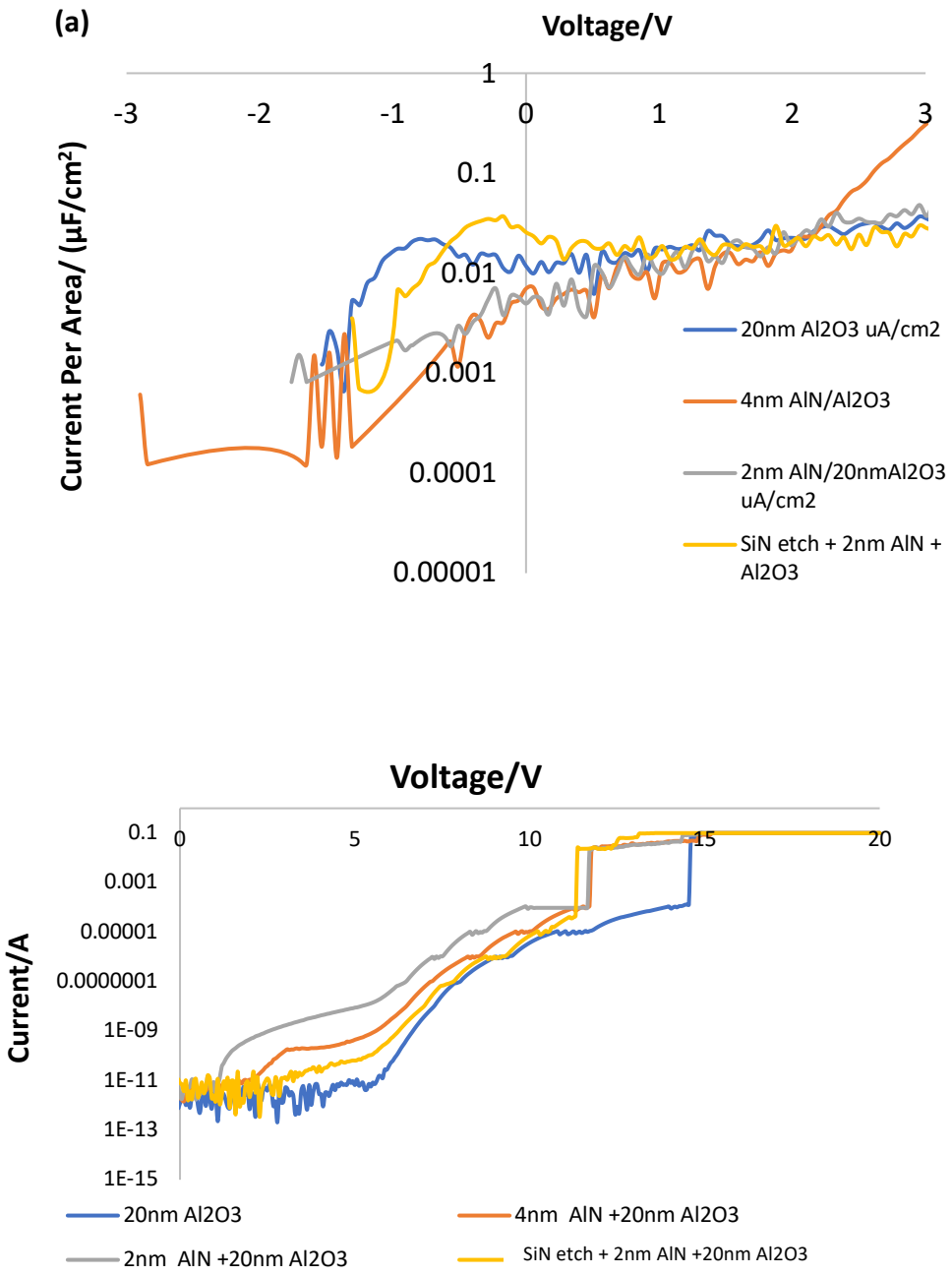



**Figure 7.4.13: (a) Comparative leakage currents and (b)Comparative breakdown data between samples with only 20nm Al2O3 2nm and 4nm AlN/$Al_2O_3$ gate stacks and samples that underwent an in-situ etch + 2nm AlN/$Al_2O_3$ ALD deposition**

# 7.5 Summary

A route to the realization of GaN MOS-capacitors (MOSCAPs) with an atomic layer deposited aluminium nitride (AlN) interlayer between GaN and aluminium oxide ($Al_2O_3$) using a FlexAl ALD system has been reported. The effect on growth rate and refractive index of AlN of various parameters were optimised and finally the films were chosen to be deposited at $300^0$C using trimethylaluminium (TMA) and $N_2$ and $H_2$ plasma with a ratio of 1:2, plasma exposure time of 20s, TMA exposure time of 20ms, TMA and plasma purge time of 3s, plasma power of 200W and pressure of 15mTorr.

The physical characterisation by XPS of these films indicates the presence an AlN. CBO of 2.04 eV and VBO of 0.6 eV were obtained between the AlN and GaN. The lower offset values compared to those reported in the literature could be a result of the impurities present in the AlN film such as carbon and oxygen that were detected, and also impurities at the GaN surface.

A summary of the electrical data is shown in table 7.5.1. All the samples used for the electrical characterisation were first subjected to an $N_2$ 150W 5min plasma pre-treatment. The samples that had an AlN interlayer were followed by in-situ ALD of a 20nm $Al_2O_3$ thermally grown at $200^0$C using TMA and $H_2O$. The C-V hysteresis and frequency decreased by 75% for samples with 2nm AlN compared to sample that only had $Al_2O_3$, the leakage current decreased by 40% and an increase in 33.3% in the slope of the C-V was achieved. The enhancement at the interface between $A_{l2}O_3$ and GaN is encouraging for the realisation of high performance GaN power transistors.

Comparisons between samples containing the sample C (2nm AlN/$Al_2O_3$ gate stack) and sample A (containing only $Al_2O_{3)}$ show better interface properties for sample C. However, these results have not been translated on to the samples using layer structure 2 where the GaN surface was never exposed to the atmosphere, sample D. Higher hysteresis, dispersion and leakage were obtained for these latter films. The $SF_6$ plasma that is used to etch the $SiN_x$ layer may have terminated the GaN surface with fluorine, which would cause poor nucleation of the AlN film. There may also be residues of Si still present on the GaN surface. The samples with the in-situ etch therefore may need an additional plasma cleaning process prior to the AlN deposition to remove surface impurities.

Further analysis needs to be carried out in-situ to confirm if the deposition of the oxide film post AlN also produce oxygen and carbon in the AlN layer.

| | 20nm $Al_2O_3$ | 4nm AlN/ 20nm | 2nm AlN/20nm $Al_2O_3$ | In-situ SiN etch+ 2nm AlN/20nm $Al_2O_3$ |
|---|---|---|---|---|
| $\Delta_{Hysteresis}$/ mV | 200 | 50 | 50 | 500 |
| $\Delta_{Dispersion}$/mV | 200 | 150 | 50 | 500 |
| dc/dv ($\mu F/cm^2.V$) | 0.119 | 0.137 | 0.164 | 0.133 |
| Leakage at ($1V/\mu A/cm^2$) | 0.016 | 0.0088 | 0.0096 | 0.023 |
| Breakdown voltage/ V | 14.6 | 11.6 | 11.6 | 11.3 |
| Breakdown electric field ($Mv/cm^2$) | 7.3 | 4.8 | 5.3 | 5.1 |

**Table 7.5.1: summary of electrical data**

# 7.6 Reference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7. Knoops, H. C. M., De Peuter, K. & Kessels, W. M. M., "Redeposition in plasma-assisted atomic layer deposition: Silicon nitride film quality ruled by the gas residence time", *Appl. Phys. Lett.* **107,** (2015).
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# 8. Complete in-situ processing

## 8.1 Introduction

The metal-dielectric interface is of equal importance to that of a semiconductor-dielectric interface since it determines the threshold voltage of completed transistors [1]. Defect states at the metal-dielectric interface can contribute to changes in the threshold voltage**.** The roughness of a metal-oxide interface can also contribute to high leakage and decrease in the dielectric constant of the insulator [2]. Gate electrode roughness at the oxide/gate interface can also cause enhanced localized electric field intensity at the gate-oxide interface [2].

During fabrication, at high enough temperatures metal can diffuse into the dielectric resulting in mobile ions. The metal electrode can also intermix at the metal-dielectric interface and reduce the overall dielectric constant of the oxide [2]. ALD deposited metal gates are conformal and achieve pristine dielectric/metal interfaces, so can avoid these issues.

The chapter examines the effect of a "complete in-situ" gate process on the electrical performance of GaN MOS-capacitors. The starting semiconductor materials are the "in-situ" $SiN_x$ capped GaN epi-structures described in Chapter 6. In the work reported in this chapter, the in-situ $SiN_x$ cap is removed in the plasma etch chamber of the cluster tool described in Chapter 6, and then transferred under vacuum into the atomic layer deposition (ALD) chamber of the cluster tool, where an $N_2$ plasma pretreatment is performed and $Al_2O_3$ is deposited, as described in detail in Chapter 6. As both dielectrics and metals can be deposited by ALD, there is the potential to directly follow the deposition of the gate dielectric with titanium nitride deposition by a plasma enhanced atomic layer deposition (PE-ALD) technique. This is the "complete in-situ" approach.

Two different precursors which have been used to deposit TiN are titanium chloride ($TiCl_4$) and tetrakis-dimethylamino titanium (TDMAT) [3]. $TiCl_4$ releases HCl ($3TiCl_4 + 4NH_3 \rightarrow 3TiN + 2HCl + 1/2N_2$) as a by-product which is corrosive to other films. The HCl can also combine with $NH_3$ to produce amino salts which are non-volatile and can become embedded in the TiN films, which can increase the resistance of the films [3]. Due to these drawbacks, TDMAT has been used as the precursor in this work.

TiN can be deposited using TDMAT with either $NH_3$ or $N_2$ and $H_2$ plasma. The overall reaction using $NH_3$ is show in reaction 8.1 to 8.3[4].

$$Ti(N(CH_3)_2)_4 + 4/3NH_3 \rightarrow TiN + 4HN(CH_3)_2 + 1/6N_2 \quad 8.1$$

Where the ALD half reactions include:

$$2NH^* + Ti(N(CH_3)_2)_4 \rightarrow N_2Ti(N(CH_3))_2^* + 2HN(CH_3)_2 \quad 8.2$$

$$N_2Ti(N(CH_3)_2)_2^* + 4/3NH_3 \rightarrow N_2TiNH_2^* + 2HN(CH_3)_2 + 1/6N_2 \quad 8.3$$

Where the Asterix include the surface species.

The major concern with using TDMAT however is that it can cause carbon impurities to be present in the TiN films, which can lead to increased resistance of the films. It has been reported that a mixture of $N_2$ and $H_2$ plasma with optimised gas flow rates can produce films with lower carbon content and therefore lower resistivity [5]. Thus, the TiN film deposited in this work used TDMAT and a combination of $N_2$ and $H_2$ plasma.

The MOS capacitors are used to characterise the impact of different thicknesses of TiN (10 and 20nm) initially. These films were deposited with a vacuum break between the oxide and TiN deposition so that the electrical data obtained from these sample can also be compared to samples where the TiN was grown without a vacuum break. The thickness with the most favourable electrical characteristic is then used to examine the effects of a complete-in-situ process.

## 8.2 Experimental Details

The experiments used to evaluate the effect of an in-situ deposited TiN gate were carried out on 15x15mm GaN samples grown by MOCVD with the layer structure shown in Figure 6.2.1 **in** chapter 6**.** The samples were cleaned using a standard ultrasonic clean in acetone for 5 minutes, before being rinsed in isopropropanol (IPA) and then in RO water. As described previously in chapter 6, the samples were first transferred to the etching chamber where the $SiN_x$ was etched using reactive ion etching (RIE) in an $SF_6$ plasma for 45 seconds at 50W, 50mTorr and 50 sccm. Following this the samples were transferred under vacuum to the ALD chamber, where an $N_2$ plasma pre-treatment at 150W for 5 minutes was performed followed by deposition of 20nm of thermal $Al_2O_3$ at $200^0$C using trimethyl aluminium (TMA) and water. TiN was then deposited using tetrakis(dimethylamido)

titanium (TDMAT) and $N_2$ and $H_2$ plasma at $350^0$C, 200W, 15 second plasma exposure time and 15:5 sccm $N_2$:$H_2$ gas flow ratio. Between the oxide and TiN deposition, the ALD chamber was preconditioned with 30 cycles of TiN.

To investigate the effects of the thickness of deposited TiN, film thicknesses of 10nm and 20nm were deposited on GaN MOSCAP samples that had 20 nm thermal $Al_2O_3$. All the samples used for this investigation underwent the in-situ $SiN_x$ etch, pretreatments and ALD $Al_2O_3$ before being taken out of the chamber. The chamber was then preconditioned with 30 cycles of TiN and each sample was loaded separately to deposit different thicknesses. Therefore, there was a vacuum break between the $Al_2O_3$ and TiN depositions on these samples. The effect on electrical properties of TiN film thicknesses was validated by examining the C-V and I-V properties. The thickness providing the most favourable electrical characteristics was chosen and this was compared with a complete in-situ process where there was no vacuum break between the $Al_2O_3$ and TiN depositions. This was executed by transferring the sample back to the etching chamber during the ALD chamber precondition. The sample was then transferred back to the ALD chamber afterwards to deposit TiN.

The layer structure of the MOS capacitor with the oxide and the TiN film is depicted in Figure 8.2.1. The MOS capacitor fabrication process flow is shown in Appendix A**.** The following section describes the electrical data obtained for the TiN films that were deposited as described above.


**Figure 8.2.1: Layer structure of the MOS capacitor with $Al_2O_3$ and TiN film**

# 8.3 Electrical Analysis

The following subsections explain the impact on electrical data of different thickness of TiN and the impact of an in-situ deposited TiN gate. Here the term ex-situ is used to refer to the samples where there was a vacuum break between the $Al_2O_3$ and TiN deposition and in-situ is used to refer to the samples that had no vacuum break.

**Sheet resistance and resistivity**

The sheet resistance of the TiN was evaluated using the Transfer Line Method (TLM). These measurements were used to extract the sheet resistance ($R_{sh}$) and resistivity of the TiN deposited. The TiN layer was deposited on top of a 20nm $Al_2O_3$ layer to ensure that there is no conduction between the GaN and TiN. 20nmTi/ 200nm Au contacts were deposited to make contact to the TiN layer.

Table 8.3.1 summarises the results that were calculated from the measurements. The sheet resistance obtained are comparable to those in literature [5][6]. However, they are much higher than the resistivity values used for other materials as gate metal electrodes (<400μΩ/sq).

| 20nm | | 40nm | |
|---|---|---|---|
| $R_{Sheet}$ (Ω/sq) | ρ(μΩ/cm) | $R_{Sheet}$ (Ω/sq) | ρ(μΩ/cm) |
| 494.6 | $0.989 \times 10^3$ | 94.5 | $0.378 \times 10^3$ |

**Table 8.3.1: Summary of Contact and Sheet Resistances**

**Thickness validation**

TiN thicknesses of 10 and 20nm were deposited ex-situ on $Al_2O_3$ films and their C-V and I-V properties were measured at room temperature. Table 8.3.2 summarises the data measured for the different TiN thicknesses – the full set of graphs for this work can be found in Appendix B.

Shown in Table 8.3.2 is the variation of flat band voltage with TiN thickness. It can be observed that the flat band voltage varied with the thickness deposited and a 45.5% increase in the $V_{fb}$ was achieved when the film thickness increased from 10nm to 20nm. The change in $V_{fb}$ with film thickness is similar to that reported previously [7]. It has also been reported that the initial growth of TiN films is in the form of islands and the film isn't uniform [8]. Therefore, the difference in $V_{fb}$ may be due to that fact that in the 10nm films the work function doesn't represent the actual bulk value of TiN**.**

A 23.8% reduction in leakage current and a 7.35% increase in breakdown voltage is observed when the TiN film thickness is increased from 10 nm to 20 nm. However, no significant change in hysteresis, dispersion, accumulated capacitance, permittivity and C-V slope are observed when comparing 10nm and 20nm films. Based on the leakage current and breakdown voltage data, a 20 nm TiN gate metal thickness was chosen to explore the impact of a complete in-situ process.

| | **10nm** | **20nm** |
|---|---|---|
| $V_{flatband}$/(mV) | -550 | -300 |
| $\Delta_{hysteresis}$/mV | 350 | 350 |
| $\Delta_{Dispersion}$/mV | 150 | 150 |
| $C_{acc}$/(μF/cm$^2$) | 0.34 | 0.34 |
| $\varepsilon_r$ | 7.68 | 7.68 |
| (dC/dV)/(μF/cm$^2$.V) | 0.215 | 0.225 |
| $I_{leak}$/(μA/cm$^2$) at 1V | 0.008 | 0.0061 |
| $V_{br}$/(V) | 13.6 | 14.6 |

**Table 8.3.2: Summary of the effect on electrical data of different thicknesses of TiN**

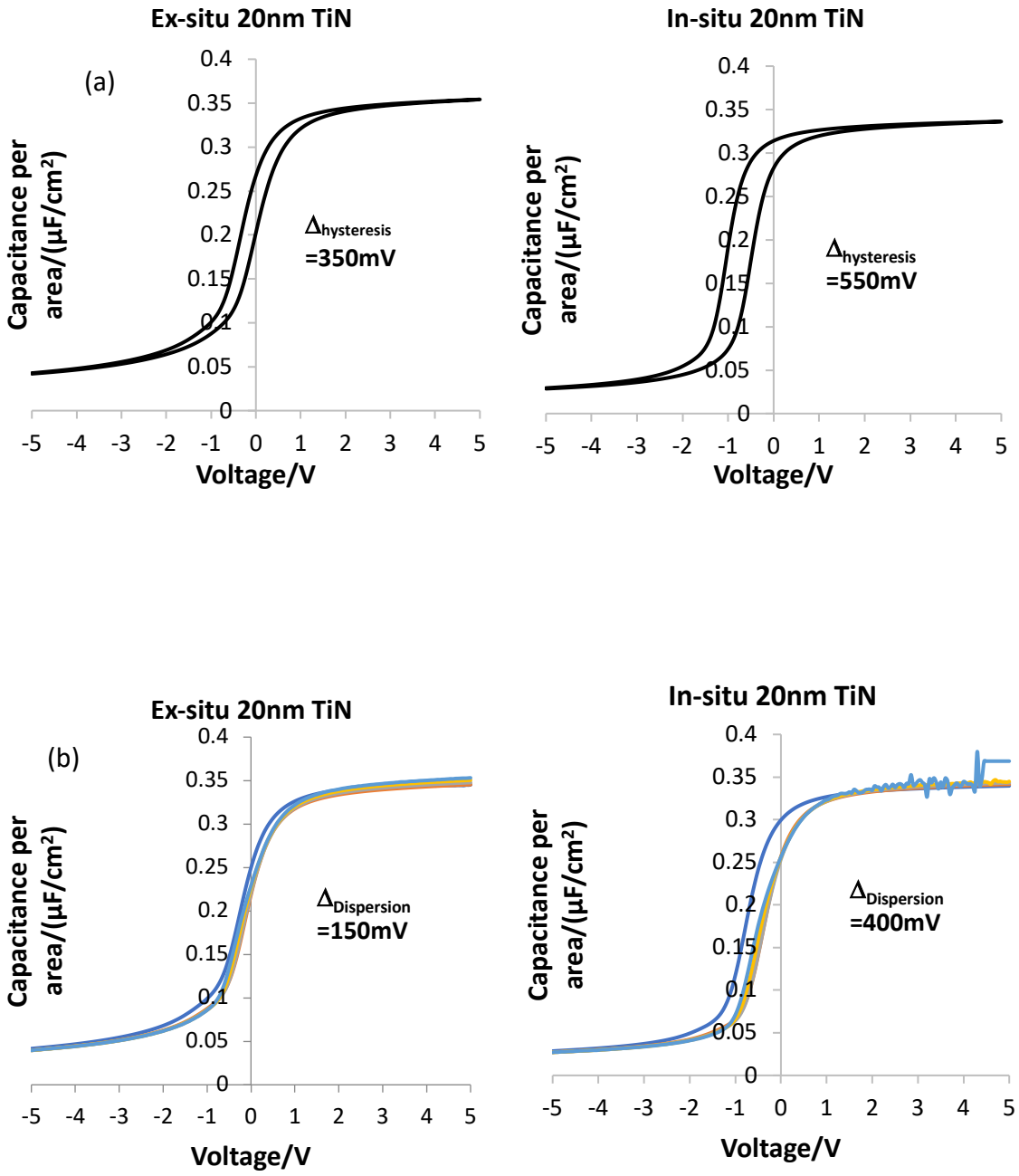
**Comparison of in-situ vs ex-situ deposited TiN**

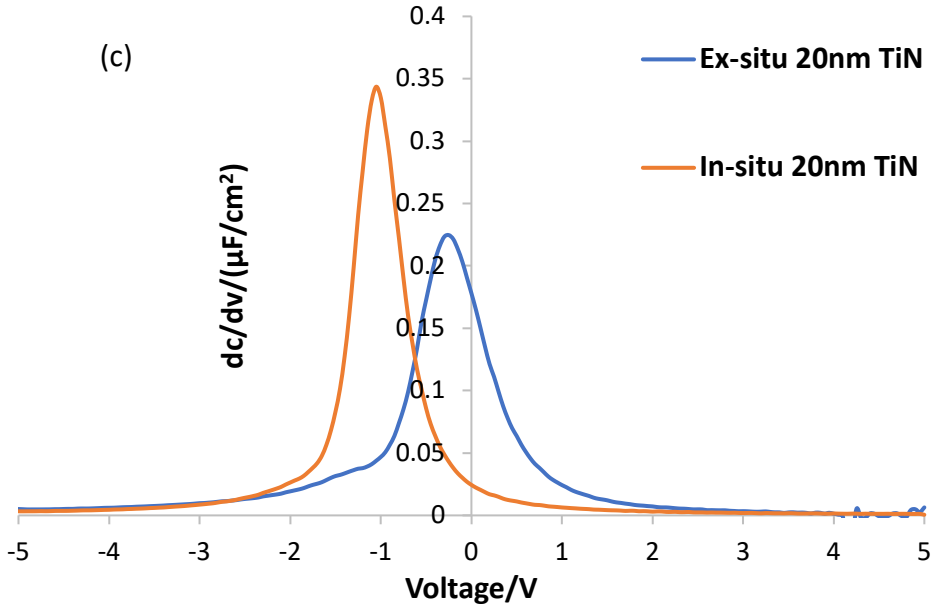
Here the in-situ SiN capping layer grown in the final step of the wafer growth process has been removed in the etching chamber using the $SF_6$ process. The sample is subsequently transferred under vacuum to the ALD reactor where an $N_2$ 150W, 5 minute plasma

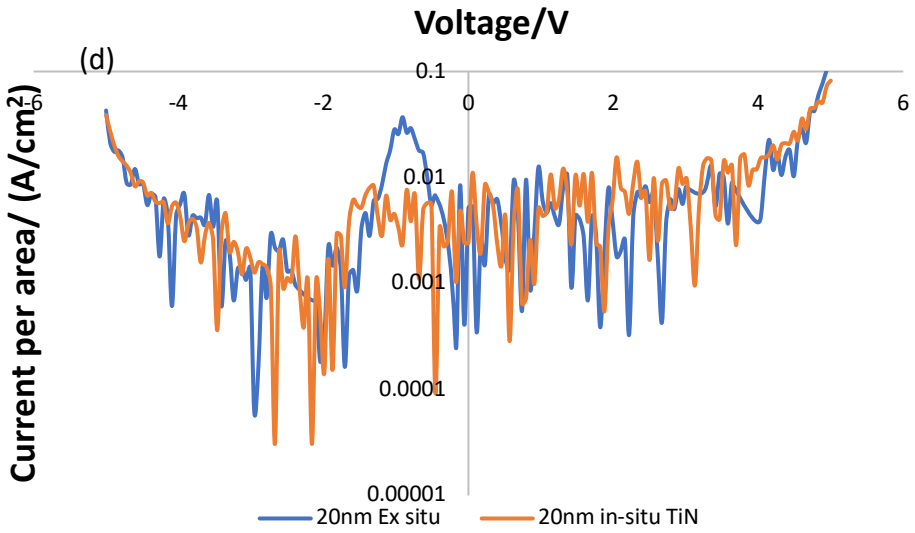
pretreatment was performed and 20nm of thermal $Al_2O_3$ was deposited. This was followed by deposition of a PE-ALD 20nm TiN film after preconditioning of the ALD chamber. The electrical data summarised in Table 8.3.3 compares the data between samples where the TiN was deposited with and without a vacuum break between the oxide and TiN deposition. The electrical data measured of these samples are illustrated in Figures 8.3.1(a) to (e). A substantial difference is seen in the slope of the C-V curve from the MOS capacitors realised by the two processes. The slope of the in-situ deposited TiN sample is 55.6% higher than that of the ex-situ deposited TiN sample, indicative of a reduction in interface state density. Further, the leakage current of the in-situ deposited TiN samples was 29.5% lower and the breakdown voltage was 16.4% higher than the ex-situ deposited TiN samples. In contrast, the in-situ deposited TiN process resulted in increases in both the C-V hysteresis and frequency dispersion as shown in Figure 8.3.1(a) and (b). The $\Delta_{hysteresis}$ is 57.1% higher and the $\Delta_{Dispersion}$ is 167% higher in the in-situ deposited TiN samples in comparison with the ex-situ samples. It can also be observed in Figure 8.3.1(d) that there is a peak in leakage curves of the samples containing 20nm ex-situ deposited TiN. It is unclear what has caused this ans it requires further investigation.

| | **20nm TiN with vacuum break** | **20nm TiN with no vacuum break** |
|---|---|---|
| $V_{flatband}$/(mV) | -300 | -1050 |
| $\Delta_{hysteresis}$/mV | 350 | 550 |
| $\Delta_{Dispersion}$/mV | 150 | 400 |
| $C_{acc}$/(μF/cm$^2$) | 0.34 | 0.34 |
| $\varepsilon_r$ | 7.68 | 7.68 |
| (dc/dv)/(μF/cm$^2$.V) | 0.225 | 0.35 |
| $I_{leak}$/(μA/cm$^2$) at 1V | 0.0061 | 0.0043 |
| $V_{br}$/(V) | 14.6 | 17 |

**Table 8.3.3: Summary of the effect on MOS capacitors on electrical data of in-situ and ex-situ deposited TiN gates**


Ex-situ 20nm TiN
(a)
Capacitance per area/(µF/cm²)
Voltage/V
Δhysteresis =350mV
In-situ 20nm TiN
Δhysteresis =550mV
(b)
Ex-situ 20nm TiN
Δdispersion =150mV
In-situ 20nm TiN
Δdispersion =400mV


(c)
Ex-situ 20nm TiN
In-situ 20nm TiN
dc/dv/(µF/cm²)
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
-5
-4
-3
-2
-1
0
1
2
3
4
5
Voltage/V


Voltage/V
(d)
Current per area/ (A/cm²)
0.1
0.01
0.001
0.0001
0.00001
-6
-4
-2
0
2
4
6
20nm Ex situ
20nm in-situ TiN

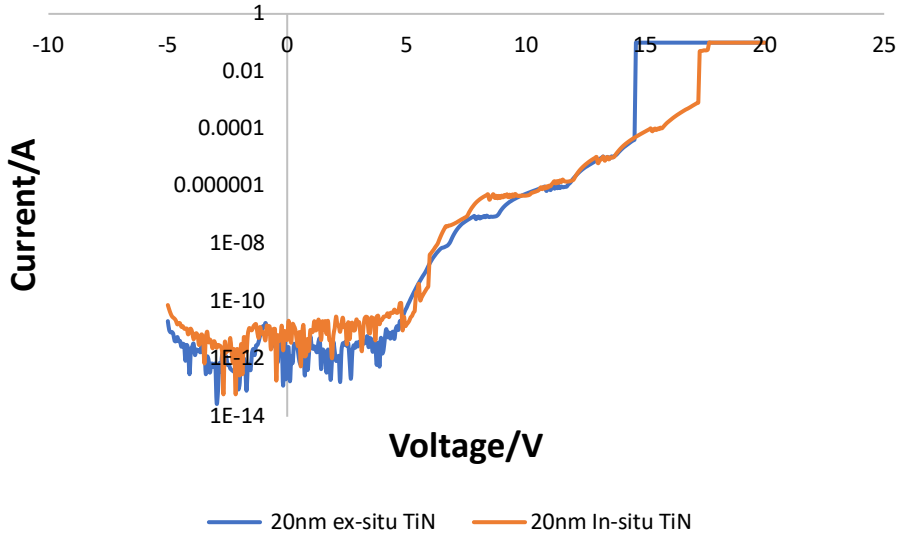



**Figure 8.3.1: Comparison of (a) C-V hysteresis data, (b) frequency dispersion data, (c) C-V slope (d) Leakage and (e) breakdown of MOS capacitor with in-situ and ex-situ deposited TiN gates**

The next section compares the effect of in-situ TiN with that of MOS capacitors deposited using Pt/Au gates.

**Comparison of MOS capacitors with Pt/Au and TiN gates**

A comparison of the electrical data obtained from Pt/Au gates before and after post metal forming gas anneal (FGA) and the in-situ deposited TiN gates is summarised in Table 8.3.4. Figure 8.3.2 illustrates the slope of the C-V curves obtained for the three samples. It can be seen that for the samples with the TiN gate, the dC/dV is 155% higher than samples with Pt/Au gates before FGA and 67.5% higher than the samples that went through an FGA. The leakage of the samples with TiN gates were 69.7% lower than of the Pt/Au gated samples before FGA and the breakdown voltage has increased by 18%.

| | Pt/Au Pre FGA | Pt/Au gates Post FGA | 20nm TiN in-situ gates |
|---|---|---|---|
| $V_{flatband}$/(mV) | -650 | 150 | -1050 |
| $\Delta_{hysteresis}$/mV | 200 | 60 | 550 |
| $\Delta_{Dispersion}$/V | 250 | 60 | 400 |
| $C_{acc}$/(μF/cm$^2$) | 0.323 | 0.320 | 0.34 |
| $\varepsilon_r$ | 7.3 | 7.23 | 7.68 |
| (dc/dv)/(μF/cm$^2$.V) | 0.137 | 0.209 | 0.35 |
| $I_{leak}$/(μA/cm$^2$) at 1V | 0.0142 | 0.0148 | 0.0043 |
| $V_{br}$/(V) | 14.4 | 14.2 | 17 |

**Table 8.3.4: Summary of comparison between ex-situ deposited Pt/Au and TiN gates**

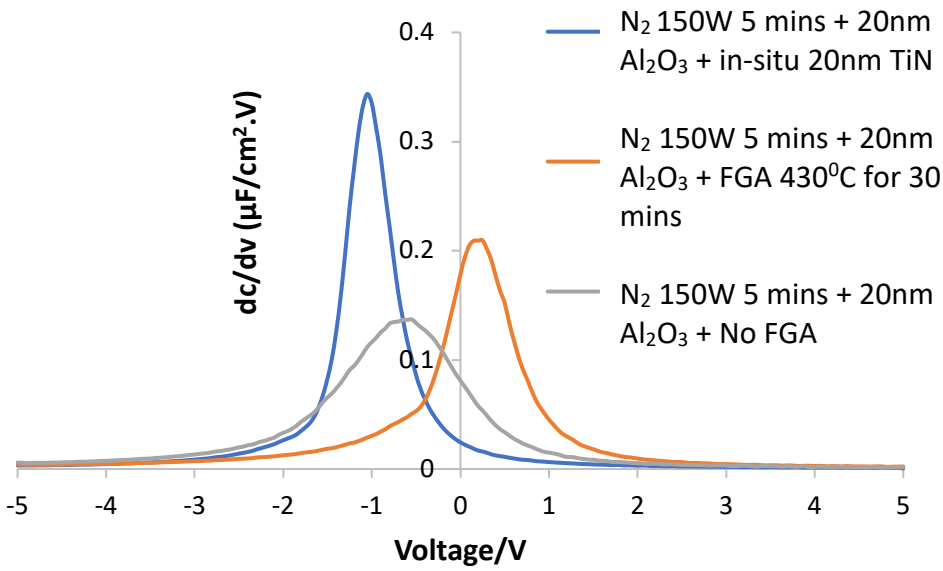



**Figure 8.3.2: C-V slope comparison between MOS capacitor sample with Pt/Au gates and in-situ TiN gate**

**Discussion**

In-situ ALD deposited TiN gates have resulted in MOS capacitors with lower leakage current, higher breakdown voltage and significantly higher dC/dV when compared with ex-situ deposited TiN samples and Pt/Au gated samples. Although high dC/dV indicates enhancements at the interface between the $Al_2O_3$ gate oxide and semiconductor, the higher $\Delta_{Hysteresis}$ and $\Delta_{Dispersion}$ data obtained from these samples indicate otherwise.

The enhancement in breakdown voltage and leakage current could be due to the $Al_2O_3$ films becoming denser as a consequence of the thermal treatment during the TiN deposition at $350^0$C for 3 hours. However, the comparison of data between the TiN films deposited with a vacuum break indicate that the improvement in leakage current, breakdown voltage and dC/dV may also be due to the $Al_2O_3$ film being protected from impurities in the atmosphere. However, the difference in flat band voltage between the in-situ and ex-situ TiN samples at this point isn't clear.

It could also be possible that an interfacial titanium oxide ($TiO_2$) or titanium oxynitrite ($TiO_xN_y$) layer has been created at the TiN/$Al_2O_3$ interface, giving rise to poor $\Delta_{hysteresis}$ and $\Delta_{Dispersion}$. The interfacial oxides should be picked up by the accumulation capacitance obtained. It has been reported that permittivity of $TiO_2$ is equal to 50 [9], using this as the permittivity the series combination of the capacitance between 20nm $Al_2O_3$ and ≈1nm $TiO_2$ would result in a capacitance of 0.32 $\mu F/cm^2$. The permittivity of $TiO_xN_y$ has been reported to be between 15 and 35 [10]. This would result in a total capacitance between 0.315 and 0.3196$\mu F/cm^2$ with ≈1nm of $TiO_xN_y$. Neither of these observations have been made in the accumulation capacitance. The high $\Delta_{hysteresis}$ and $\Delta_{Dispersion}$ could also be result of impurities from the etching chamber when then sample was transferred during preconditioning.

Further experiments are needed to clarify the impact of the thermal treatment during TiN deposition and scanning Auger data is needed to clarify the presence of elements on the $Al_2O_3$ surface when the samples have been transferred to the etching chamber. TEM data are required to show elements present within the oxide or interface.

## 8.4 Summary

Electrical evaluation of GaN MOSCAPs with different thicknesses of TiN gate metal show that 20 nm films of TiN give reduced leakage current and increased breakdown voltage when compared to devices with 10 nm TiN films. 55.6% higher dC/dV, 16.4% higher breakdown voltage and 29.5% lower leakage current are obtained from GaN MOSCAP samples with TiN gate metal that were deposited in-situ when compared to ex-situ deposited TiN films. However, a 155% higher dC/dV, 18% higher breakdown voltage and a 69.7% lower leakage current were achieved for in-situ deposited TiN samples when compared to Pt/Au samples pre FGA. The results indicate the positive benefits of including

in-situ TiN deposition, however the root cause of higher $\Delta_{hysteresis}$ and $\Delta_{Dispersion}$ in the in-situ deposited TiN films has yet to be determined and requires further investigation.

## 8.5 Reference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# 9.Conclusions and future work

## 9.1 Conclusions

Silicon transistors have been the most widely used devices in power electronics to date. However, wide band gap materials specifically gallium nitride have fundamental properties that suggest transistors realised from these materials will be able to surpass the performance of Si-based devices. In order for GaN devices to replace the technology of Si devices certain issues need to be addressed. One of the key issues adversely affecting GaN devices is the high gate leakage which can lead to lower efficiency of the device. Thus, the primary focus of the thesis has been on optimising the gate region. To reduce gate leakage, it is important that a dielectric is incorporated and it also important that the dielectric-semiconductor interface has minimum defects.

It has been reported that the surface contamination of GaN surfaces is primarily composed of oxygen, carbon and adsorbates [1]. Therefore, this work investigated a route to producing GaN devices where the GaN surface of capacitor substrates used in this work to fabricate capacitors avoided the exposure to atmosphere. This has been achieved by using GaN samples capped with a 5nm $SiN_x$ that was grown in-situ as part of the MOCVD wafer growth. A clustered plasma etch and atomic layer deposition (ALD) tool has then been used to etch the $SiN_x$ cap and transfer the substrate under vacuum to the ALD chamber where various plasma pretreatments and depositions were performed. The films deposited using ALD include $Al_2O_3$, AlN and TiN. The effect of plasma pretreatment prior to $Al_2O_3$ deposition were investigated. In addition, the effect of a post annealing treatment, forming gas anneal (FGA) has also been examined. Further, the impact of an AlN interlayer between GaN and $Al_2O_3$ and the effect of using TiN as the gate metal has been investigated. The effect of in-situ processing, pretreatments, dielectrics and metal gate have been investigated electrically by measuring their C-V and I-V properties.

- **ALD $Al_2O_3$ and Pretreatments**

The effect of $N_2$ and $H_2$ plasma pretreatments post the $SiN_x$ etch were investigated. It has been reported that a $\Delta_{Hysteresis}$ of 250mV and a $\Delta_{Dispersion}$ 310mV was reported for GaN - $Al_2O_3$ MOS capacitors that had no pretreatment but underwent a post FGA at $430^0$C for 30

minutes [2]. It can be observed from chapter 6 that the in-situ processed samples, where after the $SiN_x$ etch and no pretreatment were performed, a $\Delta_{Hysteresis}$ of 90mV and a $\Delta_{Dispersion}$ 150mV was recorded. Therefore, it can be concluded that the in-situ $SiN_x$ capped layer, has led to a reduction of 64% in the $\Delta_{Hysteresis}$ and a reduction of 51.6% in $\Delta_{Dispersion}$. This confirms the importance of a GaN surface that is unexposed the atmosphere. In comparison to all the other plasma pretreatments post FGA, the $N_2$ plasma at 150W, 5 minute produced the lowest $\Delta_{Hysteresis}$ and $\Delta_{Dispersion}$ of 60mV. It has also been demonstrated that the FGA has assisted in reducing the fixed positive charge present in $Al_2O_3$ films by shifting the threshold voltage towards the positive direction. However, the breakdown electric field of these films are between 7-7.5MV/cm, which is also lower than that achieved in literature of 9MV/cm [3]. This may be due to the contaminants such as carbon present from impurities in the ALD films. This indicates that although the interface between the oxide-GaN has improved there is yet improvements to be made in the oxide itself.

- **AlN**

An AlN ALD process was developed using trimethylaluminium (TMA) and $N_2$ and $H_2$ by checking the effect of various parameters on the refractive index and growth rate on Si. An optimised AlN film and growth process was obtained at $300^0$C gas flow ratios of 1:2, plasma exposure time of 20s, TMA exposure time of 20ms, TMA and plasma purge time of 3s, power of 200W and pressure of 15mTorr.

The physical characterisation by XPS of these films indicates the presence an AlN and a CBO of 2.04eV and a VBO of 0.6eV. The lower conduction and valence band offset values compared to those reported in the literature could be a result of the impurities present in the film such as carbon and oxygen that were also detected by XPS, and also impurities at the GaN surface.

The effect of an AlN interlayer between GaN and $Al_2O_3$ were examined electrically on bare GaN MOS capacitor samples (without an in-situ SiN cap). 4nm and 2nm AlN thicknesses were investigate, and it was concluded that the 2nm interlayer produced the best electrical data. In comparison to the sample that only had an $Al_2O_3$ layer on GaN, the sample with the 2nm interlayer reduced $\Delta_{Hysteresis}$ and $\Delta_{Dispersion}$ by 75% from 200mV to 50mV, reduced dielectric leakage current by 40% from 0.016μA/cm$^2$ to 0.0096μA/cm$^2$ and increased the

C-V slope by 33%. However, when the process was transferred to samples that had an $SiN_x$ cap at the last step of wafer growth and went through in-situ etching and ALD, the $\Delta_{Hysteresis}$ and $\Delta_{Dispersion}$ increased to 500mV. This could be due to the GaN surface being fluorine terminated by the $SF_6$ plasma used to etch the $SiN_x$ layer. The samples with the in-situ etch may need an additional plasma cleaning process prior to the AlN deposition.

- **a "complete in-situ" process using ALD TiN**

The effect of a "complete in-situ" process was examined by realising a process flow where both the GaN and $Al_2O_3$ surface was not exposed to the atmosphere. This process flow included the samples with the in-situ $SiN_x$ cap which were etched in the etching chamber, before being transferred under vacuum to the ALD chamber where an $N_2$ 150W, 5 minutes plasma pretreatment was performed and a 20nm $Al_2O_3$ layer deposited, and this was followed by a 20nm TiN ALD.

Initially two thicknesses (10 and 20nm) of TiN were grown with a vacuum break between the $Al_2O_3$ and TiN growth to examine the effect of the thickness of the TiN on electrical properties and also serve as a comparison between samples that were deposited without a vacuum break. Electrical evaluation of GaN MOS capacitors with different thicknesses of TiN gate metal showed that 20 nm films of TiN reduced leakage current and increased breakdown voltage when compared to devices with 10 nm TiN films. No difference was seen in their $\Delta_{hysteresis}$ and $\Delta_{Dispersion}$ which were 350mV/cm$^2$ and 150mV/cm$^2$ respectively. A 20nm TiN was then deposited another sample without a vacuum break, a 55.6% higher dC/dV, 16.4% higher breakdown voltage and 29.5% lower leakage current are obtained from GaN MOSCAP samples with TiN gate metal that were deposited in-situ when compared to ex-situ deposited TiN films. A 155% higher dC/dV, 18% higher breakdown voltage and a 69.7% lower leakage current were achieved for in-situ deposited TiN samples when compared to Pt/Au samples pre FGA. The results indicate the positive benefits of in-situ TiN deposition, however the root cause of higher $\Delta_{Hysteresis}$ and $\Delta_{Dispersion}$ in the in-situ deposited TiN films has yet to be determined and requires further investigation.

It can be concluded from the data of $Al_2O_3$-GaN MOS capacitors in chapter 6 that a $SiN_x$ layer where the GaN surface was not exposed to the atmosphere has been beneficial. The AlN interlayer between the GaN surface and $Al_2O_3$ on bare GaN MOS capacitor samples show considerable improvements when compared with samples with no interlayer.

Although this process didn't transfer directly on the samples that went through the in-situ etch process, further examination can be made with a different pretreatment on these samples. The high dC/dV values obtained from MOS capacitors with TiN gate metal indicate positive benefits of the in-situ TiN deposition, however further investigation is required to understand the high $\Delta_{Hysteresis}$ and $\Delta_{Dispersion}$ produced in these samples.

## 9.2 Future Work

- The MOS capacitors need to be measured repeatedly to ensure that the electrical data measured such as $\Delta_{Hysteresis}$ and $\Delta_{Dispersion}$ and leakage remain consistent with each subsequent measurement, ensuring reliable performance over time.
- A dielectric may breakdown with time, when a constant electric field is applied, which is less than the electric field strength of the material [4]. Therefore, it is essential to carry out Time-Dependent Dielectric Breakdown measurements (TDDB). This includes applying a constant voltage below the breakdown voltage to the gate, while recording the leakage current. This is repeated a number of times to obtain a distribution of the time to failure of the dielectrics. The distribution is then used to create reliability plots and to predict the TDDB behaviour of oxides at other voltages. This measurement would give information regarding the reliability of the AlN and $Al_2O_3$ films deposited.

- Scanning Auger analysis should to be carried out on samples with different pretreatments to understand the effect such as removal of impurities from these pretreatments on the GaN surface.

- FGA showed positive benefits for MOS capacitors with $Al_2O_3$ therefore the effect of an FGA needs to also be examined on the samples with the AlN interlayer and also the capacitors with the TiN gate metal. Surface analysis could also be carried out on samples that had the AlN interlayer after it went through the $SiN_x$ etch to understand the high $\Delta_{Hysteresis}$ and $\Delta_{Dispersion}$ produced in comparison to the bare GaN samples.

- It is important that surface analysis such as scanning Auger is carried out on the samples with TiN gate metal to understand the high $\Delta_{Hysteresis}$ and $\Delta_{Dispersion}$ that was produced from these samples. The effect of the thermal treatment from the TiN ALD deposition at $350^0$C for three hours needs to be investigated. This could be carried out by leaving

a sample after the $Al_2O_3$ deposition in the ALD chamber for three hours at $350^0$C and creating a MOS capacitor with Pt/Au gates in order to examine if the same leakage and breakdown properties as that of the TiN are achieved.

- Chemical analysis secondary ionisation mass spectrometry (SIMS) could be carried out to identify impurities such as carbon present in the $Al_2O_3$ and AlN films.

- XRD measurements are needed to understand the crystal structure of the deposited AlN films.

- Finally, the pretreatment and the gate stack (AlN/$Al_2O_3$/TiN) needs to be translated on to a device to examine its effect on important transistor parameters such as threshold voltage, gate leakage and breakdown voltage.

## 9.3 Reference

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# Appendix A

**1. Sample clean** - 5 minute ultrasonic clean in acetone, rinse with IPA and RO water, $N_2$ blow dry

**2. In-situ etching + ALD**

Etch 5 nm $SiN_x$ - $SF_6$ plasma 50mTorr, 50W, 50sccm

ALD $Al_2O_3$ or

$AlN/Al_2O_3$ - 20nm $Al_2O_3$ with TMA and $H_2O$ at $200^0$C or

- 2nm AlN at $300^0$C with TMA and $N_2$ and $H_2$ plasma

**3. Gate metal**

Metallise - 20nm Pt/ 200nm Au

**4. Ohmic metal**

| | | |
|---|---|---|
| Spin resist | - | LOR 6000rpm 30secs |
| Bake | - | 2mins at 150°C |
| Spin resist | - | S1818 4000rpm 30secs |
| Bake | - | 3 minute at 115°C |
| MA6 exposure | - | 6 secs |
| Develop | - | Develop MF319 2min 30secs and rinse in RO water |
| Ash | - | 2 minutes 50mTorr, 10w, 10sccm |
| $SiCl_4$ etch | - | 8mTorr, 200W, 25 sccm |
| Si flash | - | ICPCVD: 100w/0w, SiH4=10sccm, 5mT, 3secs, |
| Metallise | - | 10nm Mo/ 40nm Al/ 20nm Mo/ 30nm Au |
| Lift off | - | 1165 at $50^0$C overnight and rinse in RO water |

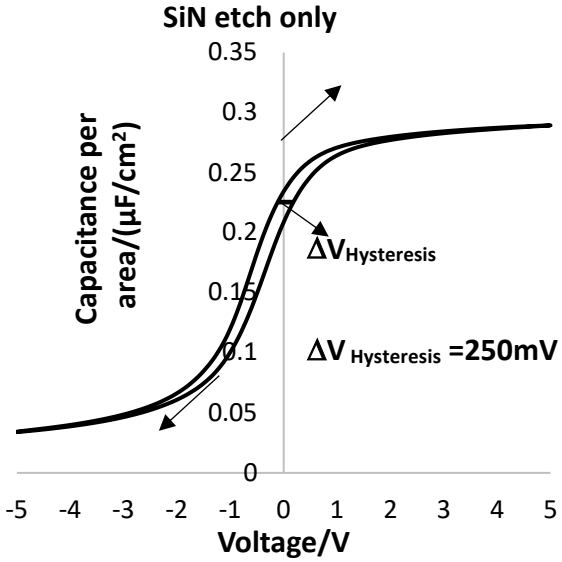
**5. Contact pad**

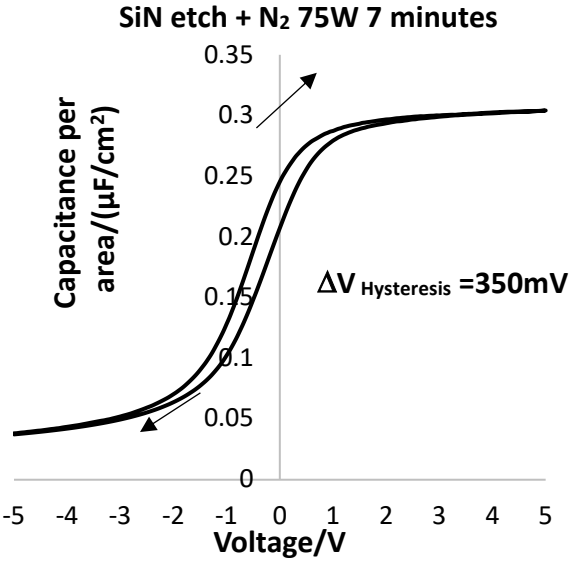
| | | |
|---|---|---|
| Spin resist | - | S1818 4000rpm 30secs |
| Bake | - | 3mins at 115°C |
| MA6 exposure | - | 6 secs |
| Develop | - | 1:1 microdev soak 75secs + Quick Rinse RO water |
| Ash | - | 2 minutes 50mTorr, 10w, 10sccm |

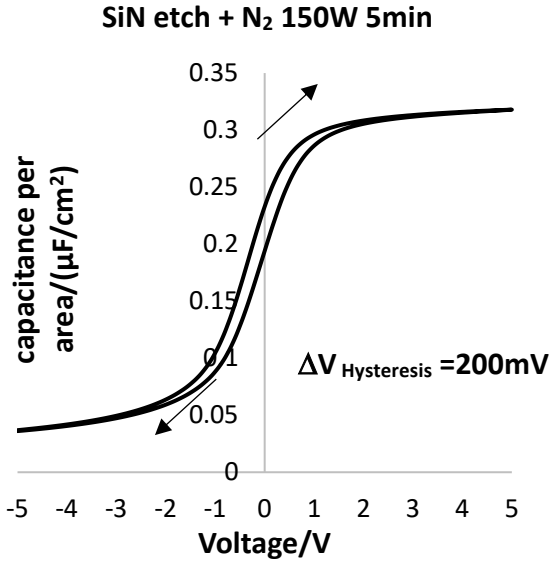
| | | |
|---|---|---|
| Metallise | - | 20nm Ti/ 200nm Au |
| Lift off | - | 1165 at $50^0$C overnight and rinse in RO water |

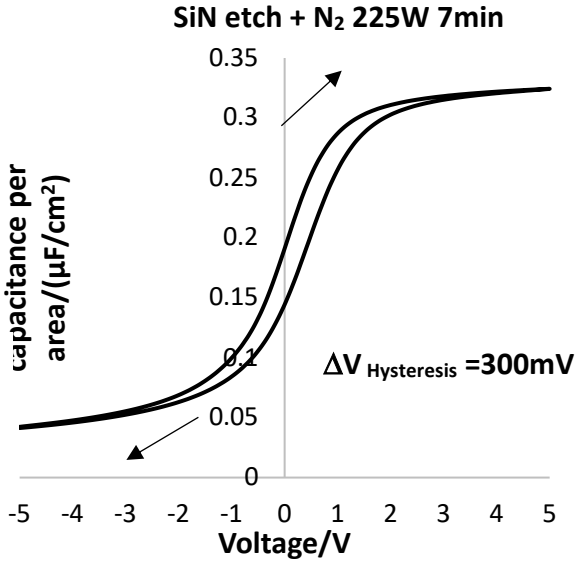
# Appendix B

- C-V hysteresis and frequency dispersion data of in-situ SiNx etching and pretreatments



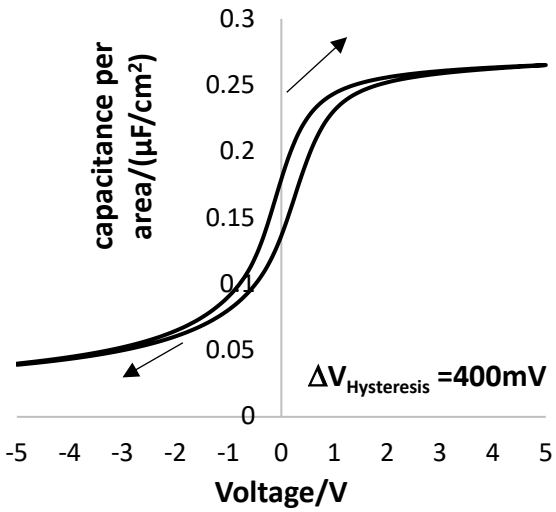



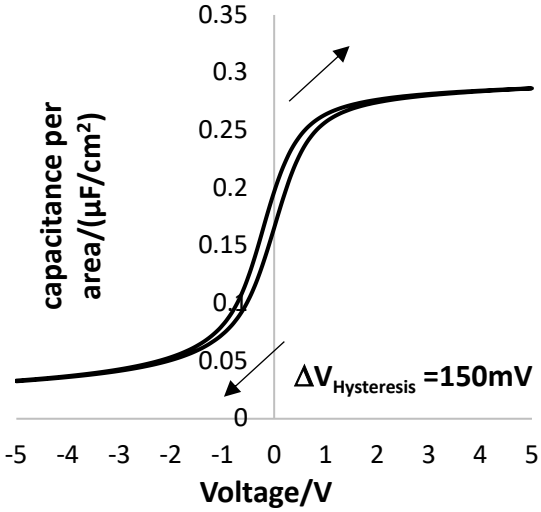



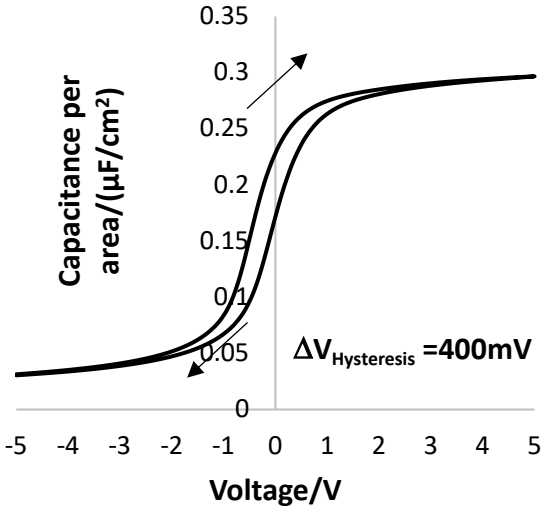

SiN etch + $H_2$ 100W 5min

SiN etch + $H_2$ 150W 3min

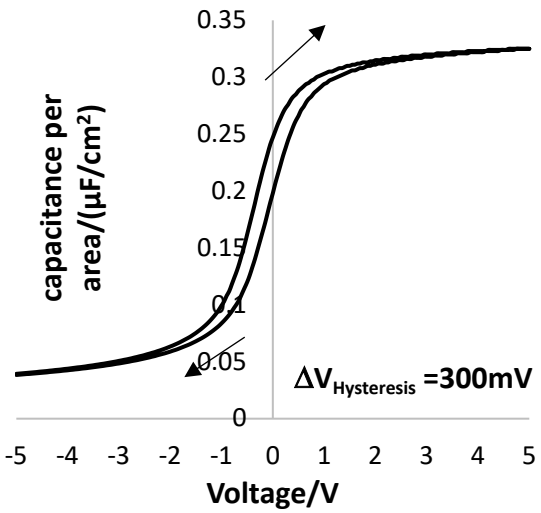


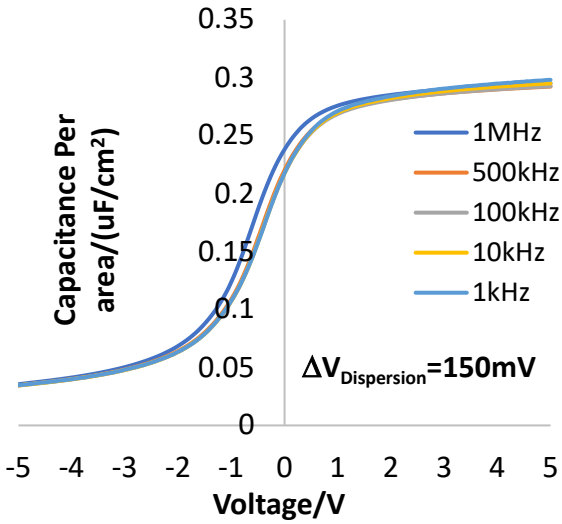

**SiN etch + $H_2$ 200W 5min**



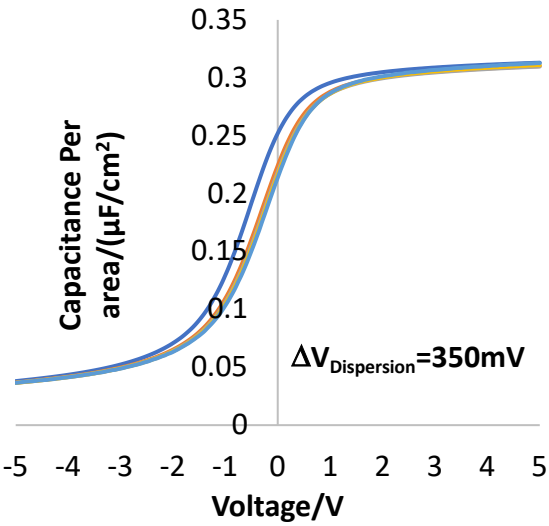

**SiN etch + $H_2$ 150W 3min + $N_2$ 150W 5min**

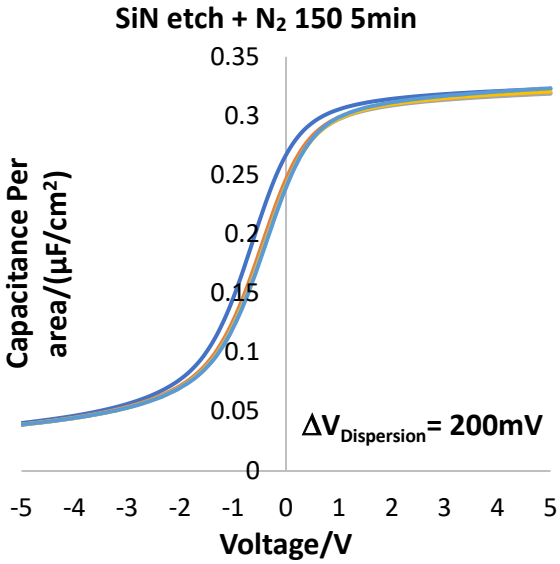


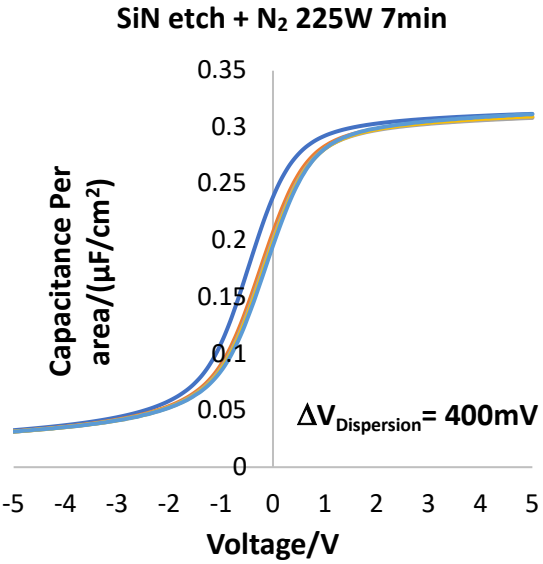

**SiN etch only**

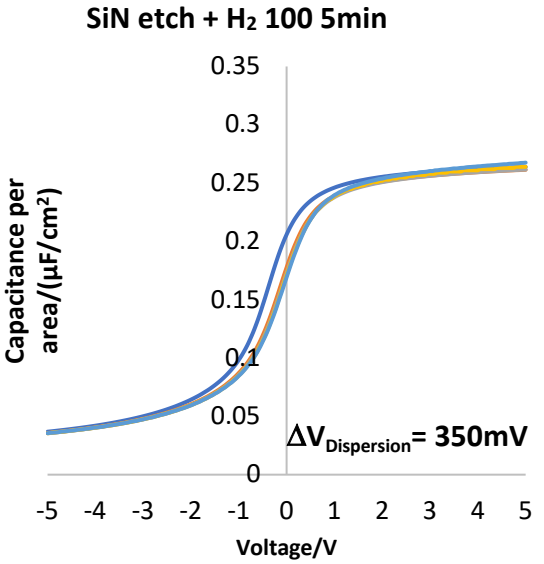


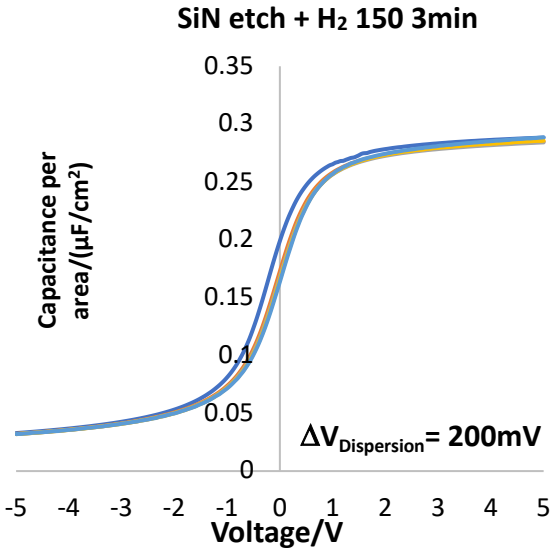

**SiN etch + $N_2$ 75W 7min**

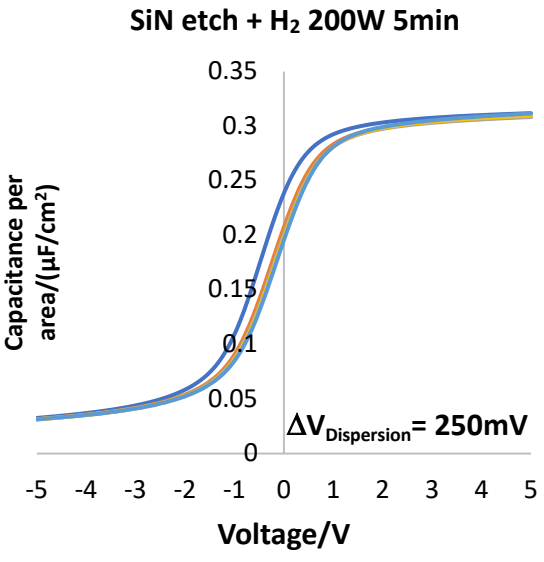


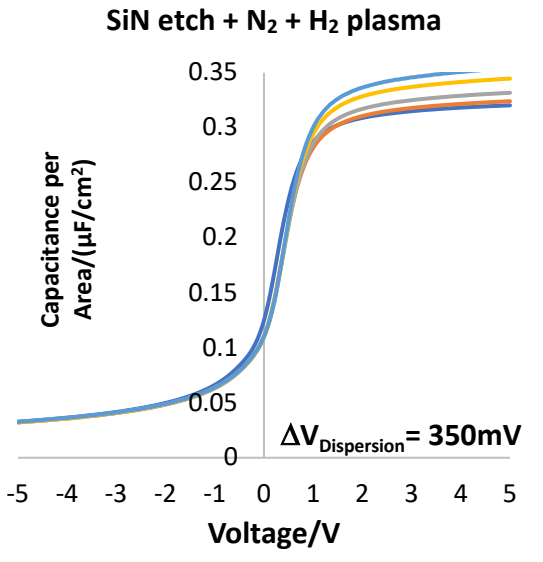

SiN etch + N2 150 5min
Capacitance Per area/(µF/cm²)
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
ΔVDispersion= 200mV
-5 -4 -3 -2 -1 0 1 2 3 4 5
Voltage/V


SiN etch + N2 225W 7min
Capacitance Per area/(µF/cm²)
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
ΔVDispersion= 400mV
-5 -4 -3 -2 -1 0 1 2 3 4 5
Voltage/V


SiN etch + H2 100 5min
Capacitance per area/(µF/cm²)
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
ΔVDispersion= 350mV
-5 -4 -3 -2 -1 0 1 2 3 4 5
Voltage/V


SiN etch + H2 150 3min
Capacitance per area/(µF/cm²)
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
ΔVDispersion= 200mV
-5 -4 -3 -2 -1 0 1 2 3 4 5
Voltage/V


SiN etch + H2 200W 5min
Capacitance per area/(µF/cm²)
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
ΔVDispersion= 250mV
-5 -4 -3 -2 -1 0 1 2 3 4 5
Voltage/V


SiN etch + N2 + H2 plasma
Capacitance per Area/(µF/cm²)
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
ΔVDispersion= 350mV
-5 -4 -3 -2 -1 0 1 2 3 4 5
Voltage/V

- Electrical data measured from MOS capacitors with 10 and 20nm TiN